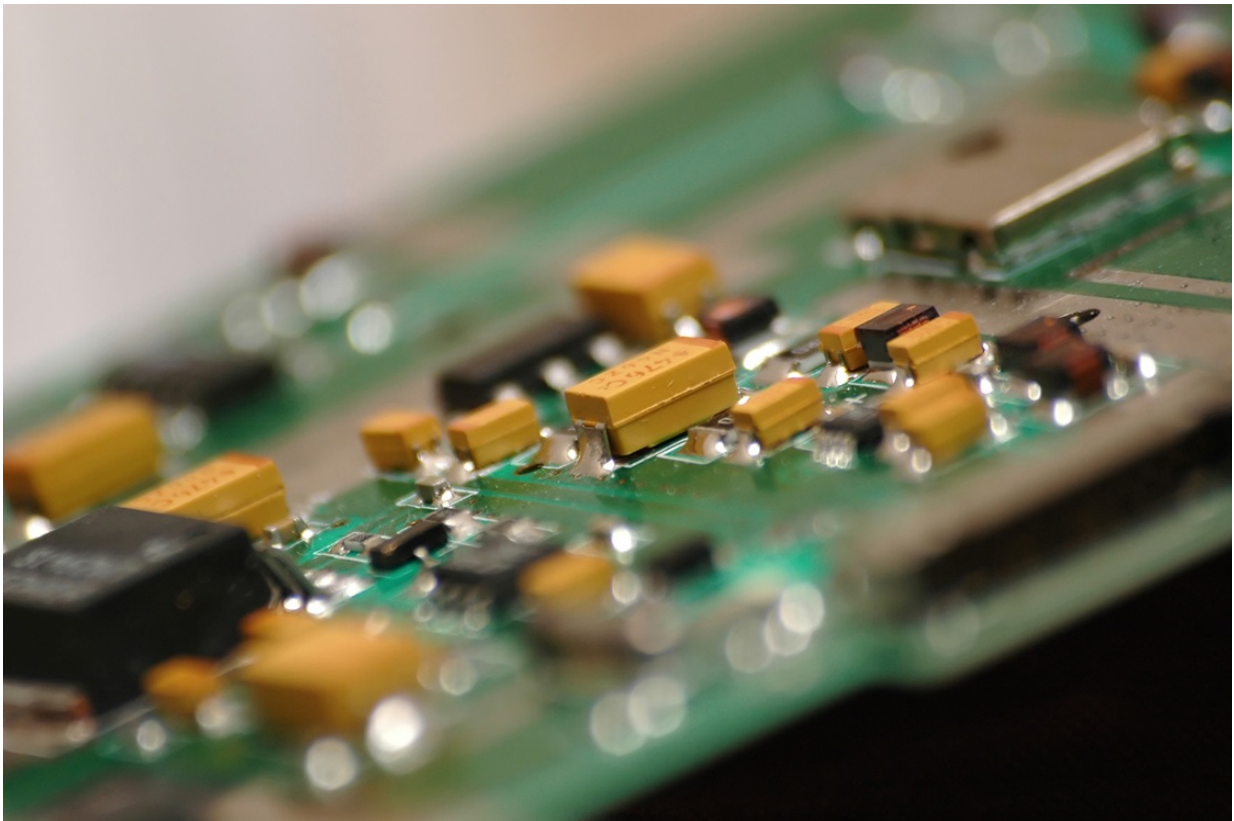# Multiplying the computing factor of algorithms on FPGA chips

July 24 2017, by Monica Westman Svenselius

Kretskort genrebild . Credit: andy_lim

Researchers at Linköping University have developed a method to increase by a factor of five the computing power of a standard algorithm performed by standard FPGA chips.

Field-programmable gate array (FPGA) chips consist of a matrix of logical gates that can be programmed in situ, and can be reprogrammed an unlimited number of times. The first FPGAs entered the market in 1985, and sales since then have increased dramatically. The market is now dominated by a couple of major players, and is expected to amount to USD $9.8 billion in 2020 (Wikipedia). The researchers have increased the processing speed of an algorithm known as the "fast Fourier transform," which is used in spectral analysis, radar technology and telecommunication.

"Until now, people have believed that once an FPGA is full, it cannot accommodate more. If you want new functionality, you have to completely rebuild the hardware, which is expensive," says Oscar Gustafsson, senior lecturer in the Department of Computer Engineering at Linköping University.

But Carl Ingemarsson, a Ph.D. student at the department, had other ideas. As an undergraduate several years ago, he was challenged to increase the speed of calculation in an FPGA. Instructors said that if the lab group could reach a frequency greater than 450 MHz, they would be excused from the final lab in the course.

"This was what was needed to convince me to examine in depth the way the logic is represented inside the chip," he says.

He achieved the frequency, skipped the final lab, and at the same time, laid the foundation for his doctoral project. The result is that FPGAs today can be made to work five times as fast or to deal with five times the number of calculations. While it's true that Carl has only confirmed this in two families of FPGA, there is no reason to believe that it is not also the case for all other families.

"This advance will save huge sums for demanding calculations in

industry, and will make it possible to implement new functionality without needing to replace the hardware," says Oscar Gustafsson.

Carl Ingemarsson's method is based on ensuring that the signal takes a smarter route through the building blocks inside the chip. "Normally, you choose an algorithm that can carry out the desired calculations, and then build up the structure, the architecture, using the required blocks. This is then transferred to the FPGA. But we have also looked at how the logic is built up, the routes the signals take, and what happens to them inside the chip. We have adapted the architecture and the mapping onto the chip using the results of this analysis."

A clever change in the signal routes gives the chip a capacity that is five times greater for each hardware unit. "It should be possible to automate this optimisation of the chip," says Carl Ingemarsson.

"At one level, it might seem that we haven't changed anything—we're still using the same standard components, but we have increased the computing power by a factor of five. This has made it has difficult to get our article published in a scientific journal," Oscar Gustafsson explains.

But the solution was so clever that someone managed to plagiarise the work before the IEEE to published it. It suddenly appeared at an IEEE conference, using copies of the diagrams, with parts of the text swapped out by completely different authors. All the support documentation in the form of original files and original diagrams was, however, available at LiU: the plagiarism was discovered, and the researcher suspended. The damage had been done, however, and publication of the original article was delayed by at least a year.