New techniques boost performance of non-volatile memory systems

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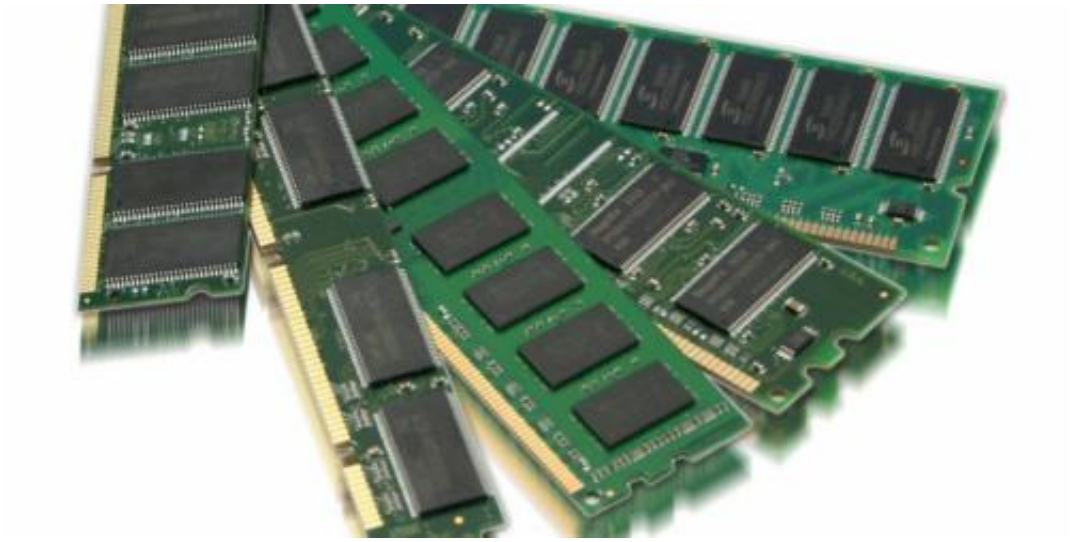

Computer engineering researchers at North Carolina State University have developed new software and hardware designs that should limit programming errors and improve system performance in devices that use non-volatile memory (NVM) technologies.

"Currently, computers rely on dynamic random access memory (DRAM) for their operations," says James Tuck, an associate professor of electrical and computer engineering at NC State and co-author of two papers on the work. "But DRAM has significant limitations, making it difficult to scale up to deal with next generation systems.

"As a result, next generation computer systems will likely rely on emerging NVM technologies for both operations and data storage. Our work here is focused on addressing some of the programming and performance challenges inherent in shifting from a DRAM computing paradigm to NVM," says Yan Solihin, a professor of electrical and computer engineering at NC State and co-author of the papers.

One challenge with NVM systems is determining how to log, or save, a chunk of memory before making changes to it. These logs allow users to reset memory if the system fails, corrupting the memory that is being modified.

At present, logging in an NVM system would require programmers to incorporate additional code into their programs – slowing performance – and increasing the number of operations that write over memory. Memory reliability suffers if it is written over too often.

To address this, researchers have developed a system called Proteus, which includes a software model and complementary hardware.

Because NVM computers are at present largely theoretical, the researchers compared the performance of Proteus against other techniques in a detailed simulator.

Other techniques wrote to memory two to six times more than Proteus, meaning Proteus was much better at preserving the long-term reliability of memory.

"Compared to existing techniques, Proteus was able to log memory almost for free, in terms of writing to memory," Solihin says.

Proteus also performed better than other techniques in terms of run speed, though the advantage there was more modest – a 9 percent to 11

percent improvement over the best existing techniques.

A second challenge with NVM systems has to do with how a system gives data an address so that it can be retrieved. Some programs require those addresses to be changed, for security and other reasons – but this can complicate programming and reduce performance in NVM systems.

To address this problem, researchers developed a hardware-driven technique that effectively creates permanent addresses for data, but allows programs to give pseudonyms to those addresses as needed.

"The programming still needs to account for the hardware, but it allows programmers to use the virtual memory approaches they're used to," Tuck says. "In simulations, our approach operated at least 1.5 times faster than previous techniques."

Papers on both new techniques will be presented at the Annual IEEE/ACM International Symposium on Microarchitecture, being held Oct. 14-18 in Boston, Massachusetts.

More information: Proteus: a flexible and fast software supported hardware logging approach for NVM. DOI: 10.1145/3123939.3124539 Presented: Annual IEEE/ACM International Symposium on Microarchitecture, Oct. 14-18, Boston, Mass.

Hardware Supported Persistent Object Address Translation, Presented: Annual IEEE/ACM International Symposium on Microarchitecture, Oct. 14-18, Boston, Mass.

Provided by North Carolina State University