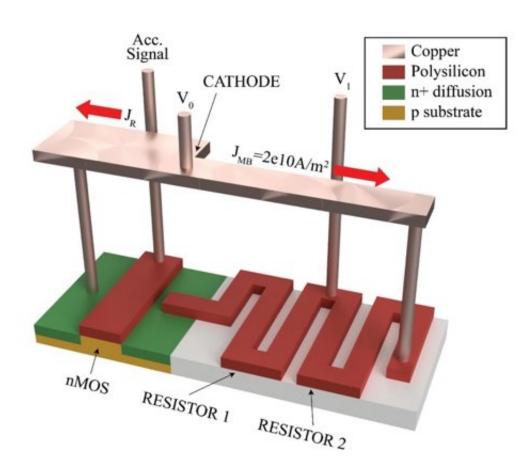


Electromigration at normal operating temperatures causes integrated circuits to fail in hours instead of year

June 13 2018, by Holly Ober



A configurable reservoir-based fast electromigration aging design for interconnects. Credit: Sheldon Tan

A University of California, Riverside engineer builds electronic circuits



just to break them as quickly as possible. A research team led by Sheldon Tan, a professor of electrical and computer engineering in the Bourns College of Engineering, has developed a new way to test the reliability of integrated circuits, such as microchips and microprocessors, that is faster than conventional techniques.

The method uses carefully controlled electromigration at normal operating temperature to cause the circuit to fail in hours instead of years, allowing researchers to assess how durable a particular manufacturing process is.

The new technique could extend the lifetime and reliability of the integrated <u>circuits</u> used in smartphones and automotive, medical, industrial, aerospace, and defense applications.

Electromigration is the top reliability concern for integrated circuits. When electrons speed through a conducting metal, they bump into metal molecules and knock them out of place. The rearrangement of molecules deforms the metal, interfering with its ability to conduct electricity and even causing wires to break. This process can take anywhere from a few minutes for some sensors to 10 years or more for very-large-scale integration (VLSI) circuits such as microprocessors.

As <u>electronic devices</u> become smaller, the metal films and wires that connect the components of integrated circuits, known as interconnects, must become finer while withstanding high densities of electrical current in order to perform with the speed and accuracy users expect. The combination elevates the risk of failure due to electromigration. Experts anticipate the electromigration lifetime to be halved with each new generation of VLSIs.

Yet, applications ranging from automatic electronics to medical devices and aerospace equipment require a long lifetime and have demanding



reliability requirements.

Developers of integrated circuits need rapid ways to test for electromigration failure before putting them into mass production for use in consumer electronics.

Conventional aging techniques involve subjecting the integrated circuit to high temperatures or high current densities, each of which can cause the circuit to fail for reasons other than electromigration, and neither of which replicates its ordinary environment or behavior.

Now, for the first time, Tan's research group has created a process that accelerates electromigration aging of interconnects in <u>integrated circuits</u> under normal working conditions.

Tan's team started with an interconnect structure designed for an electromigration lifetime of more than 10 years, as required by many electronic applications. The structure consists of a two-segment wire—one reservoir and one main branch—a cathode, and a switch to disable the reservoir. The reservoir is connected to the cathode, which directs the flow of electrons into the wire. Ordinarily, a reservoir has no electrical current and extends the life of the wire. With the reservoir disabled by the switch, however, current flows through it, stressing the cathode and causing electromigration failure in a few days instead of 10 years.

By heating the interconnect up to normal operating temperatures, less than 150°C/302°F, they reduced time to failure even more—just under two hours.

"Today's electronic devices and interconnects will become less and less reliable as technology advances. The semiconductor industry will soon face a reliability crisis if those problems are not addressed in the near



future. Our new controlled electromigration aging techniques could help to avert this crisis," Tan said.

More information: Zeyu Sun et al. Accelerating electromigration aging for fast failure detection for nanometer ICs, 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC) (2018). DOI: 10.1109/ASPDAC.2018.8297392

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