Foveros, Sunny Cove are two big markers in Intel's future
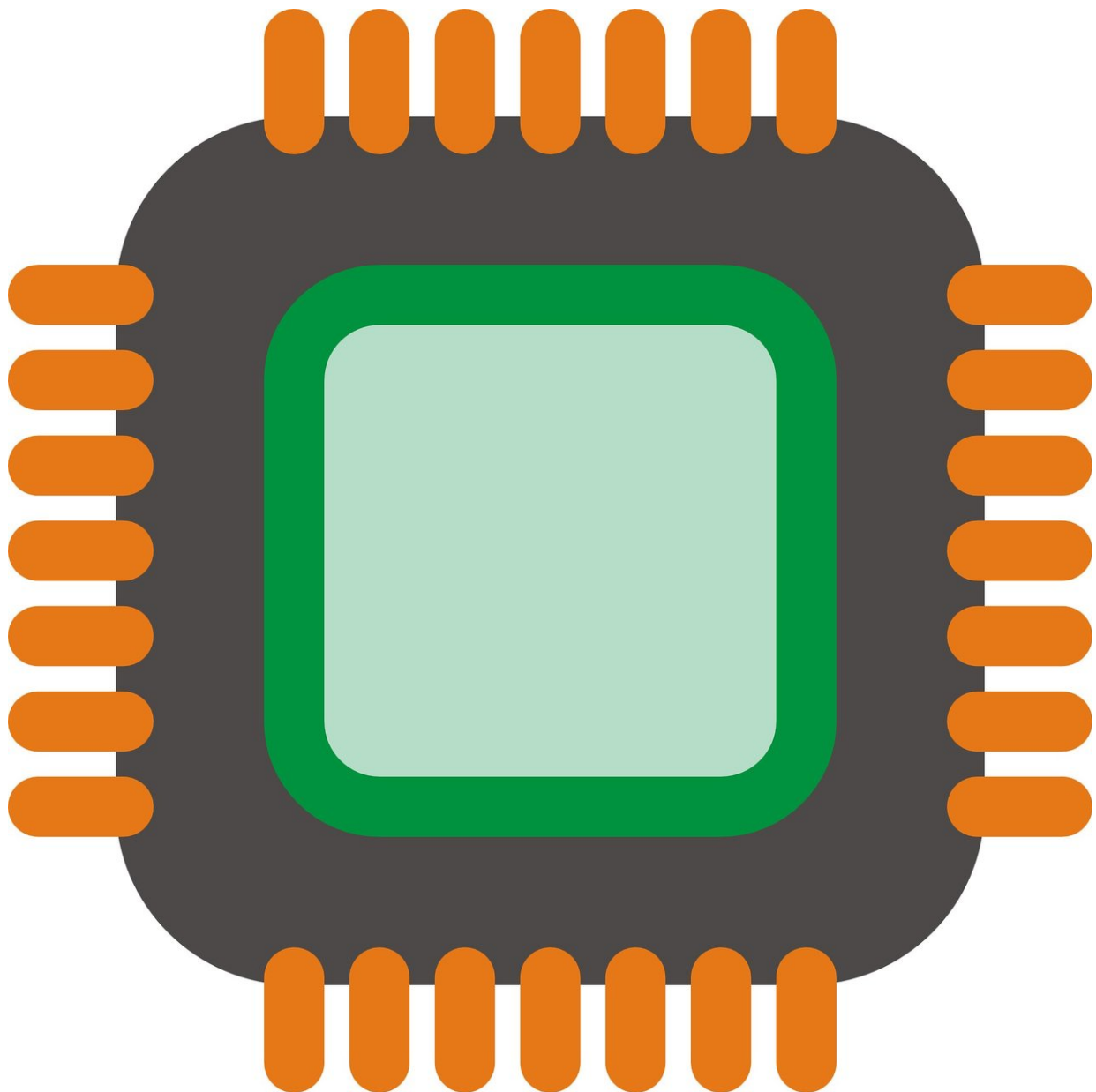
December 14 2018, by Nancy Cohen

Intel [Architecture](#) Day has come and gone but five hours of presentations have left lasting impressions that Intel is all fired up on innovation. "Intel covered a good amount of [ground](#) at the Architecture Day," wrote *AnandTech*.

The report summed up the range of new beginnings: "Intel lifted the lid on the CPU core roadmaps through 2021, the next generation of integrated graphics, the future of Intel's graphics business, new chips built on 3-D packaging technologies, and even parts of the microarchitecture for the 2019 consumer processors."

Intel demonstrated 10nm-based systems in development for PCs, data centers and networking. Mark Intel's words as roadsigns of the future: 10 nm chiplets, Foveros 3-D stacking and an enhanced microarchitecture codenamed Sunny Cove.

Can we please get inside Intel's head and figure out what they mean by "chiplets"? *The Verge*'s Vlad Savov, senior editor, said this was about "fragmenting the various elements of a modern CPU into individual, [stackable](#) 'chiplets.'"

"It's readily apparent from today's announcements that Intel has engaged in a major rethink and reorganization of its chip design strategy and [philosophy](#)," Savov wrote.

Intel's Foveros 3-D stacking approach is what grabbed Paul Lilly's attention. Lilly in *PC Gamer* said "Arguably the most interesting thing Intel announced had nothing to do with Sunny Cove or new graphics that are in the pipeline, but a new 3-D [chip](#) packaging technology called

Foveros."

What Intel unveiled is the 3-D stacking of logic chips. This enables logic-on-logic integration. The 3-D stacking technique has been used before in memory products. In Intel's design, it is especially interesting. (*The Verge*: "Intel is doing something similar with the CPU, allowing its designers to essentially drop in extra processing muscle atop an already assembled chip die.")

"The technology provides tremendous flexibility as designers seek to 'mix and match' technology IP blocks with various memory and I/O elements in new device form factors," said Intel. "It will allow products to be broken up into smaller 'chiplets', where I/O, SRAM and power delivery circuits can be fabricated in a base die and high-performance logic chiplets are stacked on top." Intel expects to launch products using Foveros in the second half of next year.

As for Sunny Cove? If you ask Gordon Mah Ung, Executive Editor, *PCWorld*, he said, "Long criticized for reusing old cores in its recent CPUs, Intel on Wednesday showed off a new 10nm Sunny Cove core that will bring faster single-threaded and multi-threaded performance along with major speed bumps from new instructions."

What's so special: He wrote that Sunny Cove cores find greater opportunities for parallelism by increasing cache sizes. The new cores will execute more operations in parallel. Compared with the Skylake architecture, the chip goes from a 4-wide design to 5-wide.

So, Savov in *The Verge* sought to tie some threads here and he posed the question, "Will Foveros 3-D stacking be part of the Sunny Cove generation of chips, or will it be something entirely separate?" The query was posed to Intel's representatives, "but the company would only say that everything 'from mobile devices to the data center' will feature

Foveros processors over time, starting in the second half of next year."

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