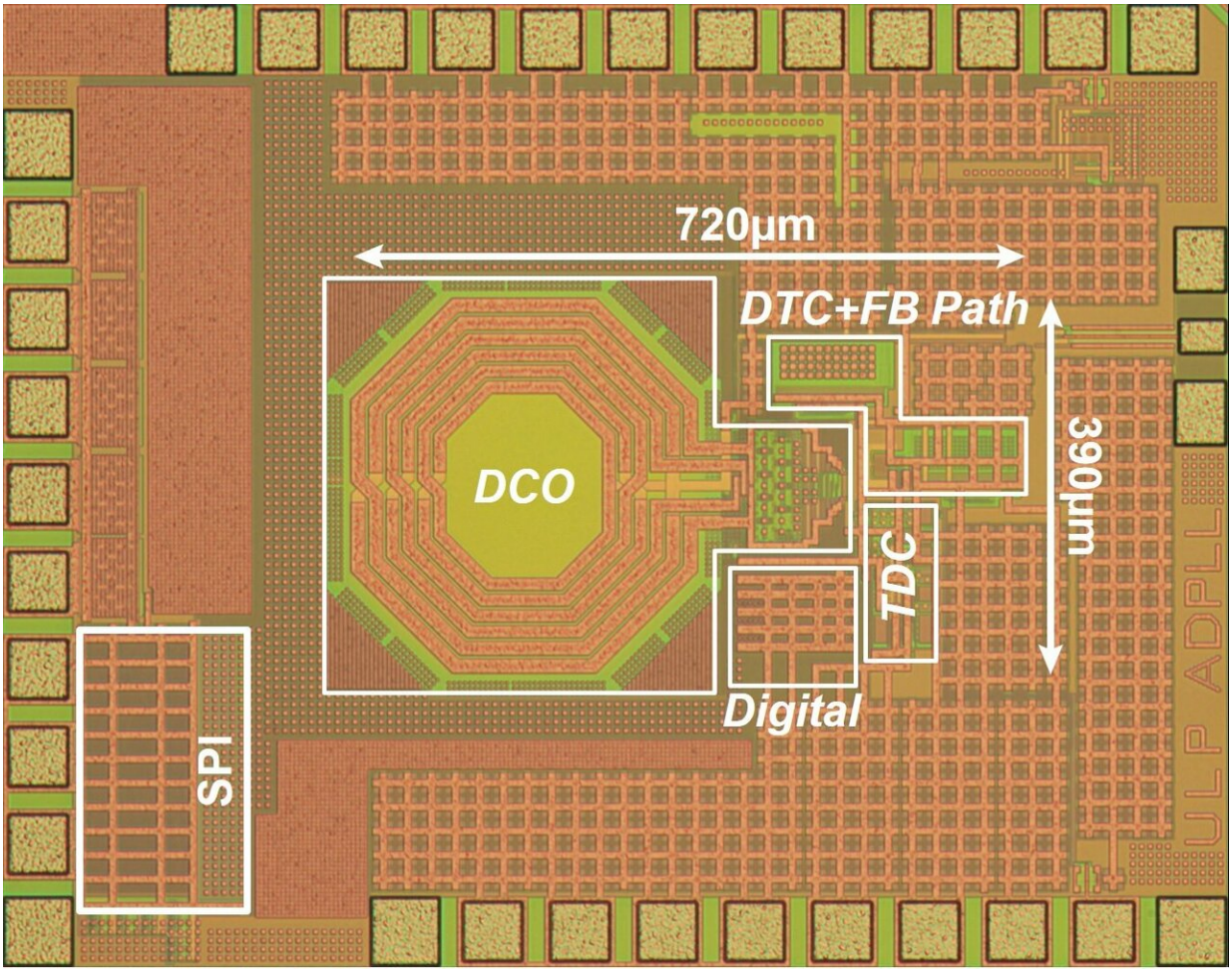
# Digital PLL achieves a power consumption of 0.265 mW

February 19 2019




The proposed fractional-N DPLL occupies an area of 0.25 $mm^2$ in 65-nanometer CMOS. Credit: Kenichi Okada

Scientists at Tokyo Institute of Technology have developed an advanced phase-locked loop (PLL) frequency synthesizer that can drastically cut power consumption. This digital PLL could be an attractive building block for Bluetooth Low Energy (BLE) and other wireless technologies to support a wide range of Internet of Things (IoT) applications.

As a key building block of wireless communication systems, frequency synthesizers need to satisfy demanding requirements. Although analog PLL frequency synthesizers have been the standard for many years, engineers in the IoT industry are increasingly turning their attention to so-called digital PLLs (DPLLs) to achieve ultra-low power operation.

Kenichi Okada, associate professor at Tokyo Institute of Technology's Department of Electrical and Electronic Engineering and his group now report a fractional-N DPLL that achieves a power consumption of only 265 microwatts (μW), a figure that is less than half the lowest power consumption achieved to date (980 μW). (Table 1)

The researchers found that overall power consumption could be greatly reduced by using an automatic feedback control system. "This automatic-switching feedback path consumes a power of 68 μW, which leads to a power consumption of 265 μW for the whole DPLL," Okada says.

The promising DPLL could go on to be used as a component for processors, memories and a vast new range of IoT devices that will be expected to be both cost-effective and eco-friendly by running on ultra-low power. Okada notes that early experiments show the DPLL could extend battery life by four times.

| | This Work | ISSCC'17 | ISSCC'14 | ISSCC'18 |
|---|---|---|---|---|
| Output Frequency (GHz) | 2.05 - 3.10 | 1.8 - 2.5 | 2.1 - 2.7 | 2.0 - 2.8 |
| Power (μW) | **265** | 673 | 860 | 980 |
| FoM (dB) | **-236.8** | -235.8 | -236 | -245.6 |

Scientists at Tokyo Institute of Technology have developed an advanced phase-locked loop (PLL) frequency synthesizer that can drastically cut power consumption. This digital PLL could be an attractive building block for Bluetooth Low Energy (BLE) and other wireless technologies to support a wide range of Internet of Things (IoT) applications. Credit: Kenichi Okada

This paper is partially based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

This work is being presented in the Frequency Synthesizers session at the 2019 International Solid-State Circuits Conference (ISSCC), the world's leading annual forum on solid-state circuits and systems-on-a-chip.

Provided by Tokyo Institute of Technology