New standard allows stacked dies in 3-D integrated circuits to connect with test equipment

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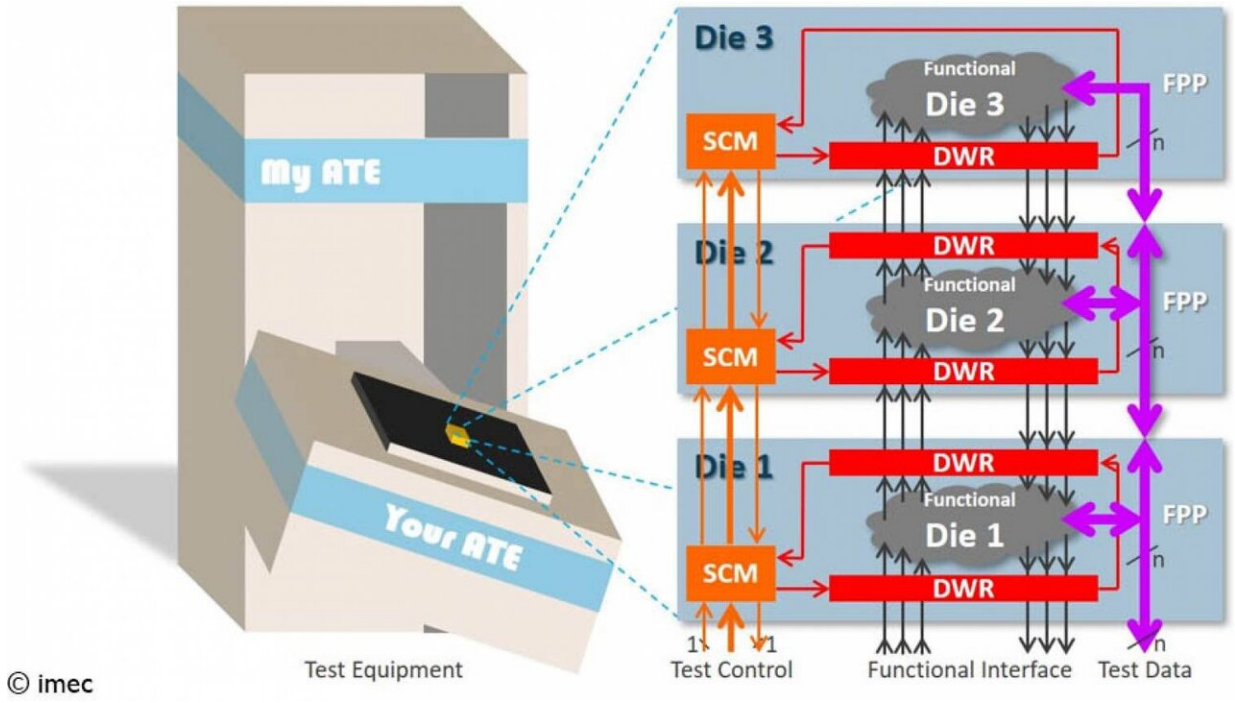

Conceptual cross-section of a 3D-IC consisting of three stacked dies. Test equipment sends test stimuli into and receives test responses from the 3D-IC's external interface located at the bottom of the stack. The IEEE Std 1838™-2019 design-for-test elements in the various dies form a consistent test access architecture through which the test equipment can access every die in the stack. Credit: IMEC

This week, IMEC, a world-leading research and innovation hub in nanoelectronics and digital technologies, announced that IEEE Std 1838TM-2019—recently approved by the IEEE Standards Association—will be included in IEEE Xplore Digital Library from February 2020 onward. The new standard allows die makers to design dies which, if compliant to this standard, constitute, once stacked in a 3-D-IC by a stack integrator, a consistent stack-level test access architecture. The standardization effort of the 3-D-DfT (design-for-test) was initiated by IMEC.

3-D-ICs exploit the vertical dimension for further integration by stacking dies on top of each other as a way of keeping the momentum of Moore's Law going. Eric Beyne, fellow and program director 3-D System Integration at IMEC, says, "Advances in wafer processing and stack assembly technologies are creating a wealth of different stack architectures. This causes a sharp increase in the number of potential moments at which testing for manufacturing defects can be executed: pre-bond (before stacking), mid-bond (on partial stacks), post-bond (on complete stacks), and final test (on packaged 3-D-ICs). Test equipment contacts ICs via its external interface through probe needles or at test socket. In a die stack, that external interface typically resides in the bottom die of the stack. For the test equipment to be able to deliver test stimuli to and receive responses from the various dies up in the stack, collaboration from the underlying dies is required to provide test access to the die currently being tested."

An IEEE working group to standardize 3-D-DfT was founded in 2011 by Erik Jan Marinissen, scientific director at IMEC in Leuven, Belgium and he served as its first chair. In recent years, Adam Cron, principal R&D engineer in the Design Group at Synopsys, has been the driving force as the current chair of the Working Group.

Amit Sanghani, vice president of engineering in the Design Group at

Synopsys in Mountain View, California, U.S. stated: "3-D-IC is an important technology to deliver the next wave of innovation as the industry scales past 7nm. Currently, die might come from different suppliers with disjoint DfT architectures.

The new standard consists of three main elements. (1) DWR, the die wrapper register: scan chains at the boundary of each die in the stack to enable modular testing of the internals of each die and of the interconnects between each pair of adjacent dies. (2) SCM, the serial control mechanism: a single-bit test control mechanism that transports instructions into the stack to control the test modes of the various die wrappers. (3) FPP, the optional flexible parallel port, i.e., a scalable multi-bit test access mechanism to efficiently transport up and down the die stack the large volumes of data typically associated with production test. While DWR and SCM are based on existing DfT standards, the FPP is truly novel to IEEE Std 1838.

Wolfgang Meyer, senior group director R&D at Cadence Design Systems in San Jose, California, U.S., says, "A DfT standard like IEEE Std 1838 is important to the industry. Die makers know what they must provide, and stack integrators know what they can expect. Moreover, EDA suppliers like Cadence can focus their tool support on architectures that are compliant with the new standard. It is good that there is some user-defined scalability with the standard as the 3-D-IC field is so wide—a rigid 'one-size-fits-all' standard would not work."

Junlin Huang, manager of a 150-person strong DfT team of HiSilicon in Shenzhen, China, says, "Per year, we do DfT insertion and automatic test pattern generation (ATPG) for tens of very large and complex digital chip designs in the most advanced technologies. Now, these products start using 3-D technology and my DfT team needs to be ready to handle the associated DfT and ATPG challenges. IEEE Std 1838 will help us with that task."

From February 2020 onward, the new standard IEEE Std 1838 will be available via IEEE Xplore to subscribers of IEEE standards as well as for purchase to everybody else.

Provided by IMEC