

# **A new design strategy to fabricate 2-D electronic devices using ultrathin dielectrics**

January 9 2020, by Ingrid Fadelli

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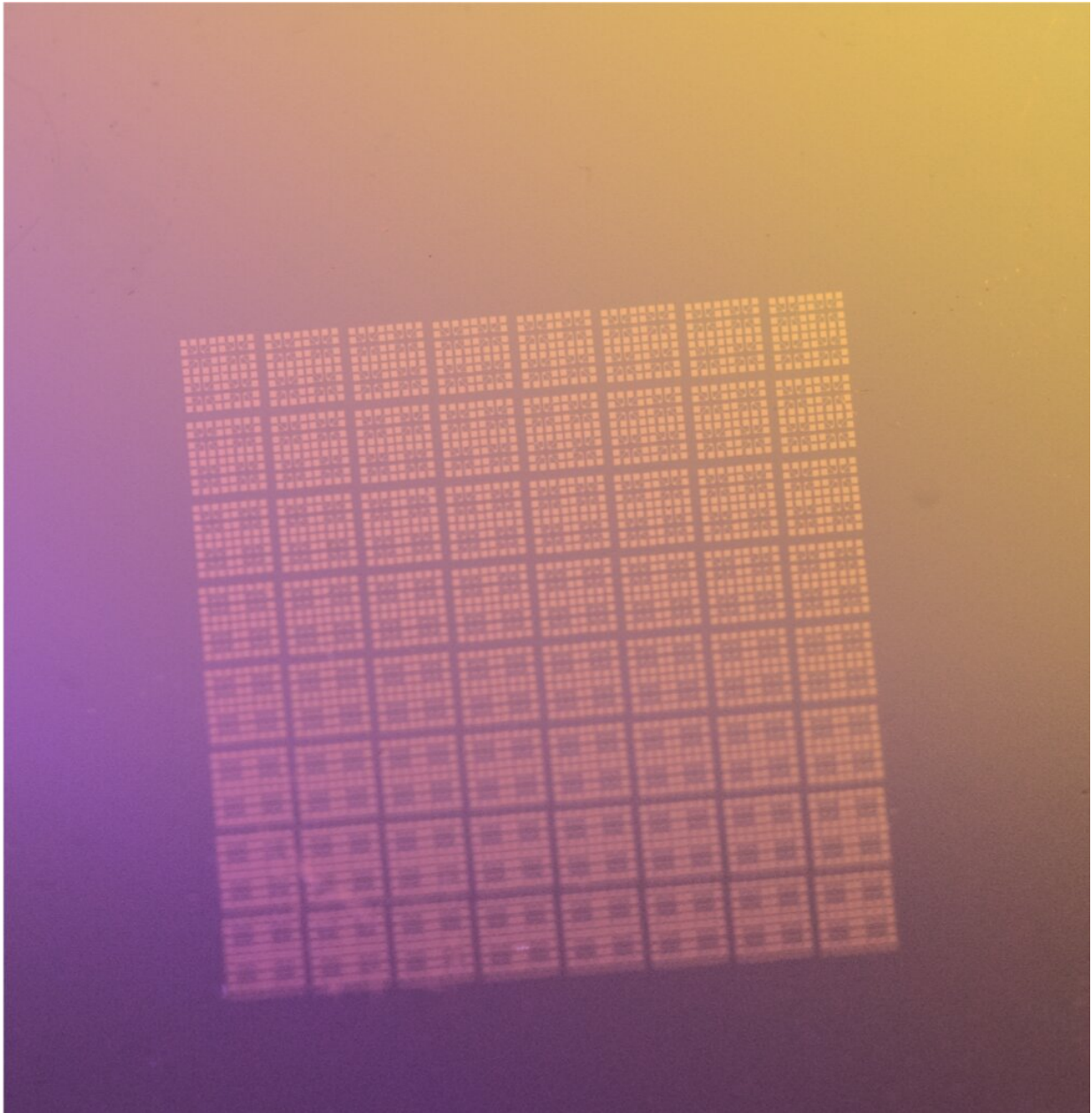


Image of a device array fabricated using the method proposed by the researchers. Credit: Li et al.

2-D semiconductors could have very useful applications, particularly as channel materials for low-power transistors. These materials display very high mobility at extreme thicknesses, which makes them particularly promising alternatives to silicon in the fabrication of electronics.

Despite their advantages, implementing these materials in transistors has so far proved to be challenging. In fact, 2-D semiconductors are of a dangling-bond-free nature; thus, it is notoriously difficult to deposit ultrathin high- $\kappa$  gate dielectrics (i.e., substances with [dielectric properties](#) or insulators) on the materials via [atomic layer deposition](#) (ALD), often resulting in discontinuous films.

Researchers at Nanjing University in China have recently presented a new strategy to overcome this limitation, ultimately allowing the deposition of gate dielectrics on 2-D semiconductors. In [a paper published in \*Nature Electronics\*](#), they reported the successful ALD of high- $\kappa$  gate dielectrics on 2-D semiconductors using a molecular crystal as a seeding layer.

"Our research tries to solve the issue of high-quality gate dielectric integration for 2-D transistors," Xinran Wang, one of the researchers who carried out the study, told TechXplore. "In state-of-the-art Si transistors, the effective oxide thickness (EOT) has been scaled down to sub-1 nm. At present, there is a big gap between 2-D materials and Si in terms of EOT, density of interface state ( $D_{it}$ ), and gate leakage. If one wants to seriously push forward 2-D transistor technology, this gap must be overcome."

The approach introduced by Wang and his colleagues enables the production of dielectrics with an equivalent oxide thickness of 1 nm on graphene, molybdenum disulphide ( $\text{MoS}_2$ ) and tungsten diselenide ( $\text{WSe}_2$ ). The dielectrics that result from the researchers' approach exhibit a reduced roughness, density of interface states and leakage when compared with those produced using more conventional methods. Interestingly, they also present an improved breakdown field.

"Other than 2-D transistors, another direction explored by my research group is organic electronics," Wang added. "Over the past several years, we have developed means to precisely control the assembly of molecules on 2-D material surface. For many molecules, including PTCDA, [we proved that we can control the growth so well that only a monolayer \(~0.3 nm\) is uniformly deposited](#), with a very clean interface."

The interface layer created by Wang and his research team in their previous work is one of the thinnest interface layers currently attainable. In their present study, they used this layer to fabricate graphene radio-frequency transistors that operate at 60 GHz, as well as  $\text{MoS}_2$  and  $\text{WSe}_2$  complementary metal-oxide-semiconductor transistors with a supply voltage of 0.8 V and a low subthreshold swing of  $60 \text{ mV dec}^{-1}$ . Finally, they also used their technique to create  $\text{MoS}_2$  transistors with a channel length of 20 nm with an on/off ratio of over  $10^7$ .

"I think our most meaningful result was that we were able to achieve 1 nm EOT in 2-D materials," Wang said. "It is widely believed that 2-D channel can reduce the power consumption of transistors compared to bulk semiconductors. However, in order to achieve that, we have to use the same operation voltage, and the transistors can be turned off sharply (subthreshold swing close to 60 mV/dec). Both quantities depend highly on the quality and thickness of gate dielectric. Our study truly demonstrates the potential of 2-D semiconductors toward low-power electronics."

Wang and his research group were the first to successfully develop 2-D transistors with a 1 nm EOT, successfully depositing [dielectric](#) on three different materials. Remarkably, the EOT and gate leakage they attained are comparable to those observed in state-of-the-art silicon CMOS, which is a significant step forward in this area of research.

"I think that there is still much room for improvement," Wang said. "For example, The Dit in 2-D [transistors](#) is still ~2 orders of magnitude higher than Si CMOS. In addition, it would be great to further reduce the EOT to ~0.8nm by using higher-k oxides. Finally, the compatibility of the materials we developed with existing CMOS processes also remains to be studied."

**More information:** Weisheng Li et al. Uniform and ultrathin high-k gate dielectrics for two-dimensional electronic devices, *Nature Electronics* (2019). [DOI: 10.1038/s41928-019-0334-y](https://doi.org/10.1038/s41928-019-0334-y)

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