Enabling battery-powered silicon chips to work faster and longer

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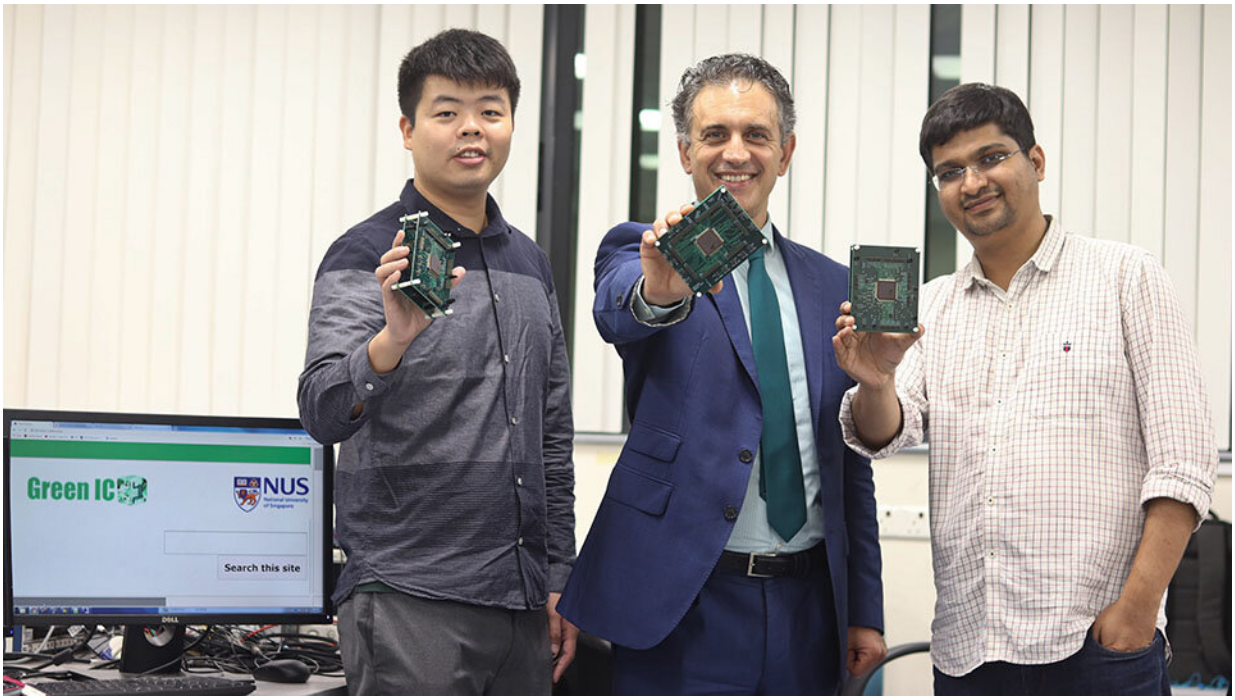


Assoc Prof Massimo Alioto (centre) and his team members Lin Longyang (left) and Saurabh Jain (right) showing off the prototyping boards for testing the silicon chips to demonstrate highly flexible power and performance, surpassing industry-standard voltage scaling. Credit: National University of Singapore

A team of researchers from NUS have invented a novel class of reconfiguration techniques that adaptively extends both the minimum power consumption and the maximum performance of digital circuits,

well beyond common voltage scaling. Such extended adaptation allows digital silicon chips to operate at lower power during normal use, and at higher performance level when necessary.

This extends the battery life under uncertain power availability in systems powered by harvesters (e.g. solar cell) or rechargeable batteries, while delivering higher peak performance to carry out on-chip data analytics upon the occurrence of events of interest. This is a key enabler for applications such as Internet of Things (IoT), artificial intelligence (AI), wearables and biomedical devices.

"Our reconfiguration techniques introduce unprecedented adaptability to fluctuating power availability and performance demand. Compared to the industry-standard voltage scaling technique, measurements on several test chips in our lab have shown that such adaptation extends the battery life of a mobile or wearable device by 1.5 times, while doubling peak performance. Our techniques can also be used to further miniaturize the battery by the same factor, while maintaining the same battery life," explained Associate Professor Massimo Alioto from NUS Engineering. He is the leader of the NUS Green IC Group that is behind this technological breakthrough.

He added, "As further benefit, the power-performance versatility of our circuit techniques allows semiconductor companies to simplify their chip portfolio and reduce the design cost, as the same digital design can be reused across a wide range of applications and markets."

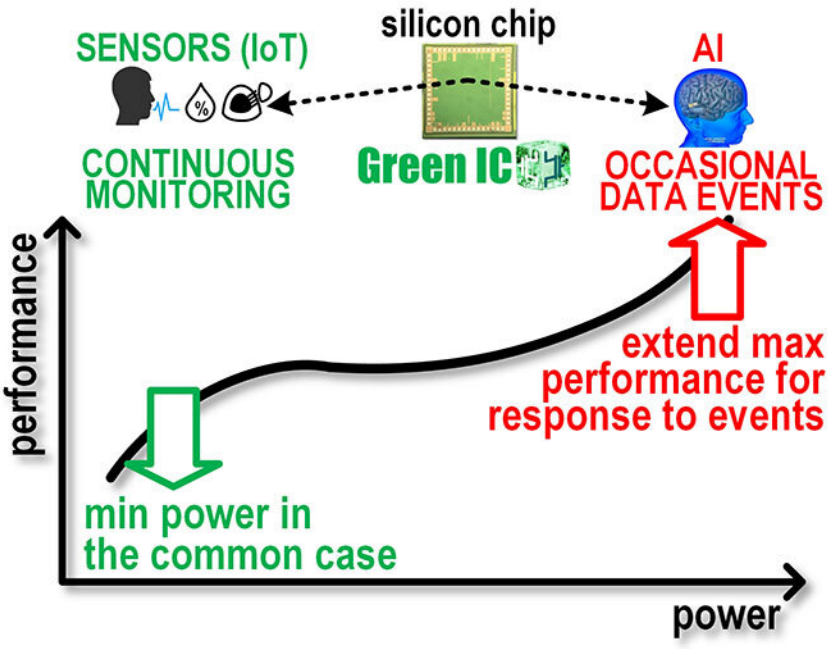
The proposed techniques have led to the demonstration of accelerators and processors (for example, Fast Fourier Transform, ARM processors) with minimum energy consumption reported to date. The research behind the novel techniques has been supported by leading semiconductor companies (Intel, TSMC) as well as the Singapore Ministry of Education and the National Research Foundation of

Singapore.

Data and clock path adaptation: Achieving both low minimum power consumption and higher peak performance

Most advanced mobile, IoT and AI applications require a flexible and wide trade-off between the average power (i.e., battery life), and the maximum performance that determines system responsiveness (e.g., when the screen is touched, or performing data analytics when a sensor produces data of interest).

Currently, dynamic voltage scaling is the gold standard in enabling such flexibility. Operating at voltages around 1 V leads to maximum performance and energy consumption, whereas reduction down to 0.4-0.5 V lowers energy consumption by four to five times and slows the operating speed by nearly 10 times. The drawback of this approach is that voltage scaling generally applies to a fixed digital architecture, although the optimal architecture for energy consumption and performance depends on the adopted voltage.



The adaptive digital circuits demonstrated by the NUS team are able to extend the battery life of intelligent silicon chips by reducing the power consumption under normal use, while scaling up performance to quickly respond to occasional data events. Credit: National University of Singapore

The NUS invention outperforms voltage scaling since its circuit reconfiguration enables better match between the architecture and the adopted voltage, and hence further reduction in energy consumption and improvements in performance at different voltages can be achieved.

Associate Professor Alioto said, "Our invention enables reconfiguration of both the "data path" where the actual processing is performed, and the "clock path" that distributes the clock signal to orchestrate the different processing tasks. In both cases, their fundamental building blocks are flexibly merged or split to create the data and clock path structure that improves either energy efficiency or performance at a given voltage."

Compared to conventional voltage scaling, the approach proposed by the NUS Green IC group makes digital circuits more versatile and adaptive, allowing simultaneous optimisation at both ends of the power-performance spectrum.

Technical book and a complete toolchain publicly available

To share the benefits of the team's new technique with both industry and research groups worldwide, a technical book has recently been released to provide the background and details of the silicon chip implementation of processors, accelerators and on-chip memories. An automated design flow has also been created and publicly released over GitHub (Please visit www.green-ic.org/).

"In our book, we introduced and demonstrated design methodologies using solely commercial design tools, which are integrated into a cohesive design flow where clock and data path reconfiguration is incorporated in a plug-and-play fashion. We are delighted to share the software code in an open-source fashion to enable massive and rapid adoption of our novel techniques in the commercial sector and in academic research," commented Associate Professor Alioto.

Next steps

The NUS research team is now looking into developing new classes of intelligent silicon systems that allow ultra-wide power-performance adaptation in AI accelerators embedded in sensing silicon chips for IoT. This will lead to next-generation systems that are always available, while being able to promptly respond to external events with very significant computational performance.

In their work, the team endeavors to enable power-performance adaptation through drop-in techniques and design methodologies in existing system architectures. This allows the achievement of power-performance benefits without disrupting the design ecosystem, thus enabling a rapid and massive adoption of next-generation intelligent systems.

Provided by National University of Singapore