User-customizable computing engine for artificial intelligence tasks

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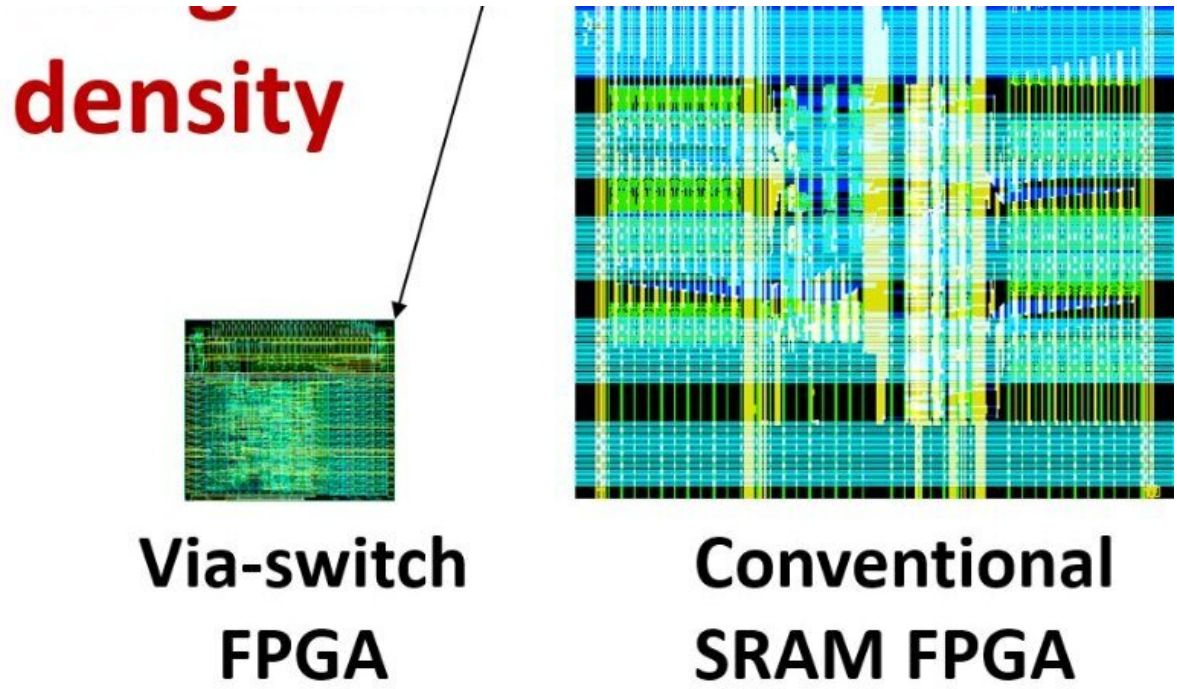

Fig. 1: Improved integration density: Comparison in integration density. Credit: IEEE International Solid-State Circuits Conference

Scientists at Osaka University have built a new computing device from field-programmable gate arrays (FPGA) that can be customized by the user for maximum efficiency in artificial intelligence applications. Compared with currently used rewireable hardware, the system increases

circuit density by a factor of 12. Also, it is expected to reduce energy usage by 80%. This advance may lead to flexible artificial intelligence (AI) solutions that provide enhanced performance while consuming much less electricity.

AI is becoming a part of everyday life for almost all consumers. Ridesharing smartphone apps like Uber, Gmail's spam filters, and smart-home devices like Siri and Nest all rely on AI. However, implementing these algorithms often requires a large amount of computing power, which means large electricity bills, as well as big carbon footprints. Systems that could be rewired to optimize the computer circuitry for each task like the human brain would provide greatly enhanced energy efficiency.

Normally, we think of hardware, which includes the physical logic gates and transistors of a computer's processor, as fixed by the manufacturer. However, field-programmable gate arrays are specialized logic elements that can be rewired in the field by the user for custom logic applications. The research team used non-volatile "via-switches" that remain connected until the user decided to reconfigure them. Using novel nanofabrication methods, they were able to pack 12 times more elements into a grid-like "crossbar" layout. By reducing the distance electronic signals need to be routed, the devices ended up needing 80% less power.

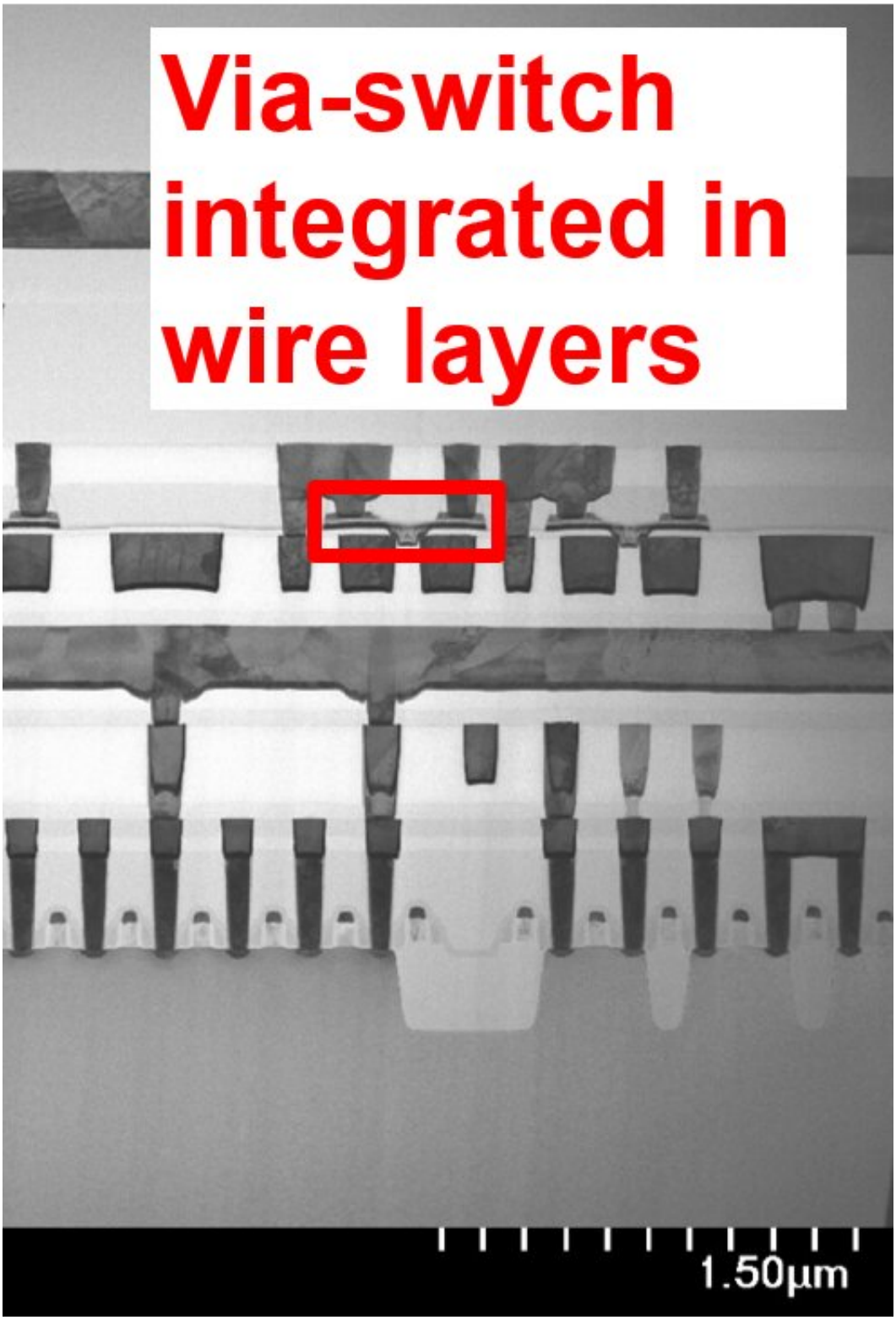

Fig. 2: Interconnect cross section of developed via-switch FPGA. Credit: IEEE International Solid-State Circuits Conference

"Our system based on field-programmable gate arrays has a very fast design cycle. It can be reprogrammed daily if desired to get the most computing power for each new AI application," first author Masanori Hashimoto says. The use of via-switches also eliminates the need for the programing silicon area that was necessary in previous FPGA devices.

"Via-switch FPGA is suitable as a high-performance implementation platform of the latest AI algorithms," says senior author Jaehoon Yu.

The article, "Via-switch FPGA: 65nm CMOS implementation and architecture extension for AI applications," was published in the technical digests of the IEEE International Solid-State Circuits Conference 2020.

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Provided by Osaka University