EPFL lab develops method for designing lower-power circuits

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An Ecole Polytechnique Federale de Lausanne (EPFL) lab has come up with a new type of logic diagram and related optimization methods, that can be used to design computer chips with a nearly 20% gain in energy efficiency, speed or size. The lab has just entered into a license agreement with Synopsys, a global leader in electronic design automation and chip fabrication software.

EPFL's Integrated Systems Laboratory (LSI) has developed a method for reducing the power requirement of computer chips by mapping out their logic flows in an entirely new way. By using a different set of logic functions for the gates on the billions of transistors on electronic circuits, this system shortens the circuits' calculation steps. That means chip designers can make their chips either smaller, faster or more energy efficient. Industry leader Synopsys has just acquired the rights to use the technology through a non-exclusive license agreement.

Streamed logic structures for more powerful chips

Today most engineers use electronic design automation software to design circuits. This software programs translate complex computational models into a labyrinth of billions of microscopic transistors. The LSI laboratory, directed by Giovanni De Micheli, has a longtime and worldwide renowned experience in design automation. There are only few companies and commercial products in use that sustain the entire semiconductor industry effort. Luca Amarù—while he was a Ph.D. student at LSI—set out to radically change how design automation software generates logic diagrams in order to produce better designs.

Amarù, who holds a doctoral degree in computer science, came up with a method that uses only two logic primitives: majority and inverter. These functions are displayed in majority-inverter graphs (MIGs). Initial studies indicated that his approach could cut the number of logic steps needed to execute a given task. Later experiments confirmed this, finding that MIG optimization reduces the number of logic levels by 18% on average relative to standard programs. That frees up transistor capacity for other tasks; engineers could also use these gains to make their chips faster or their devices smaller.

Now a senior R&D manager at Synopsys, Amarù took his findings even further. He also developed a new Boolean algebra for representing the

logic functions, which resulted in additional efficiency gains for his system.

Chips that are smaller and faster than ever before

Lab tests have shown that Amarù's method also works exceptionally well with components already in the market, such as adders and dividers. According to Mauro Lattuada, the technology-transfer manager at EPFL who arranged the license agreement, the method constitutes an important revolution: "This new way of diagraming integrated circuits not only reduces the amount of power, computing time or space needed by nearly 20%, but also gives us a new logic paradigm that can be used in other applications, such as designing and improving FPGAs [field-programmable gate arrays] or searching and analyzing data sets."

Provided by Ecole Polytechnique Federale de Lausanne

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