Researchers overcome fundamental operation challenge for voltage-controlled magnetic RAM
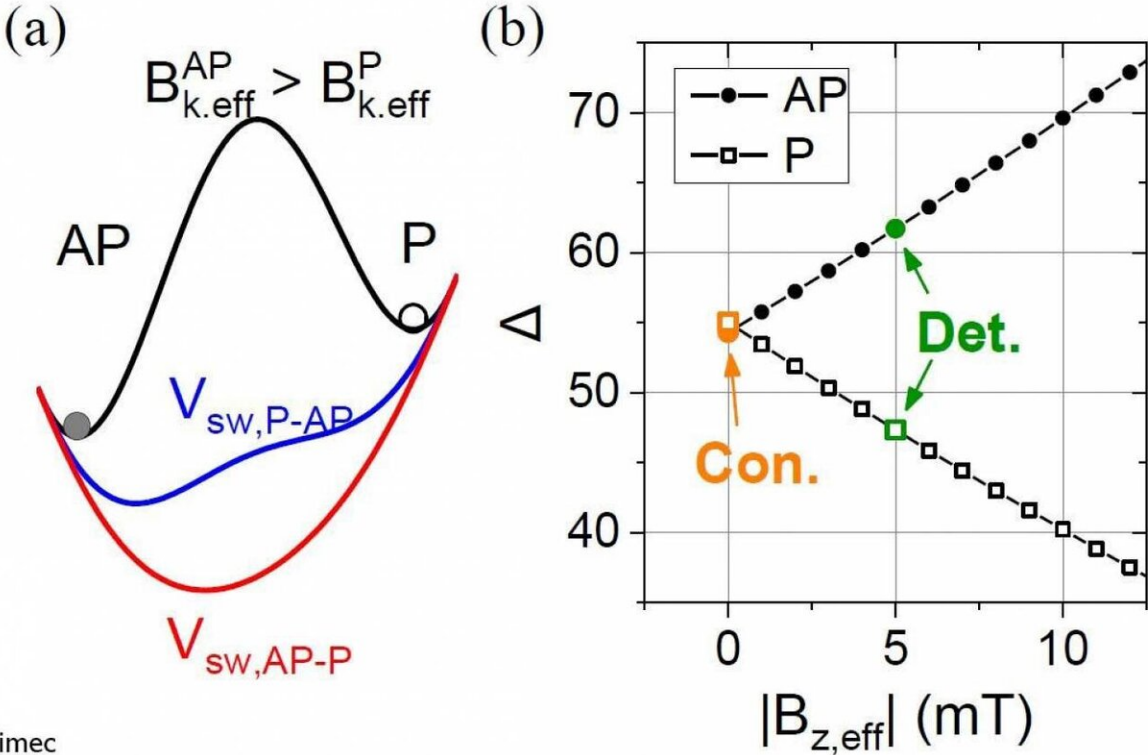
June 16 2020, by Jade Liu

Figure 1: (a) Energy diagram with Bz,eff for the proposed deterministic write, where the AP state is more stable than the P state. (b) Retention (Δ) as a function of Bz,eff. Credit: IMEC

This week, at the 2020 Symposia on VLSI Technology and Circuits,

imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, presents a deterministic write scheme for voltage-controlled magnetic anisotropy (VCMA) magnetic random access memories (MRAMs), obviating the need for pre-reading the device before writing. This significantly improves the write duty cycle of the memory, enabling ns-scale write speeds. As a second improvement, a manufacturable solution for external-field-free VCMA switching operation was demonstrated. Both innovations address fundamental write operation challenges for VCMA MRAMs, making them viable candidates for future high-performance low-power memory applications.

Voltage-controlled MRAM operation has recently been introduced to bring down the power consumption of spin-transfer-torque MRAM (STT-MRAM) devices—which is a class of non-volatile, high-density, high-speed memories.

Two basic components are required to switch from the parallel (P) to the antiparallel state (AP) (or vice versa): an electric field (across the tunnel barrier) to remove the energy barrier, and an external in-plane magnetic field for the actual VCMA switching.

Imec has now solved two fundamental operation challenges which have so far limited the write speed and manufacturability of VCMA MRAMs, respectively. The slow write operation relates to the unipolar nature of the VCMA MRAM device: the same polarity of write pulse is needed to transition from the parallel to the anti-parallel (P-AP) state as to switch from anti-parallel to parallel (AP-P) state. Therefore, the memory cell needs to be "pre-read" to know its state before writing—a sequence which significantly slows down the write operation. Imec has introduced a unique deterministic VCMA write concept that avoids the need for pre-reading: distinct threshold voltages are introduced for the A-AP and AP-P transitions by creating an offset in the energy barrier. This offset is realized by implementing a small (e.g. 5mT) offset magnetic field
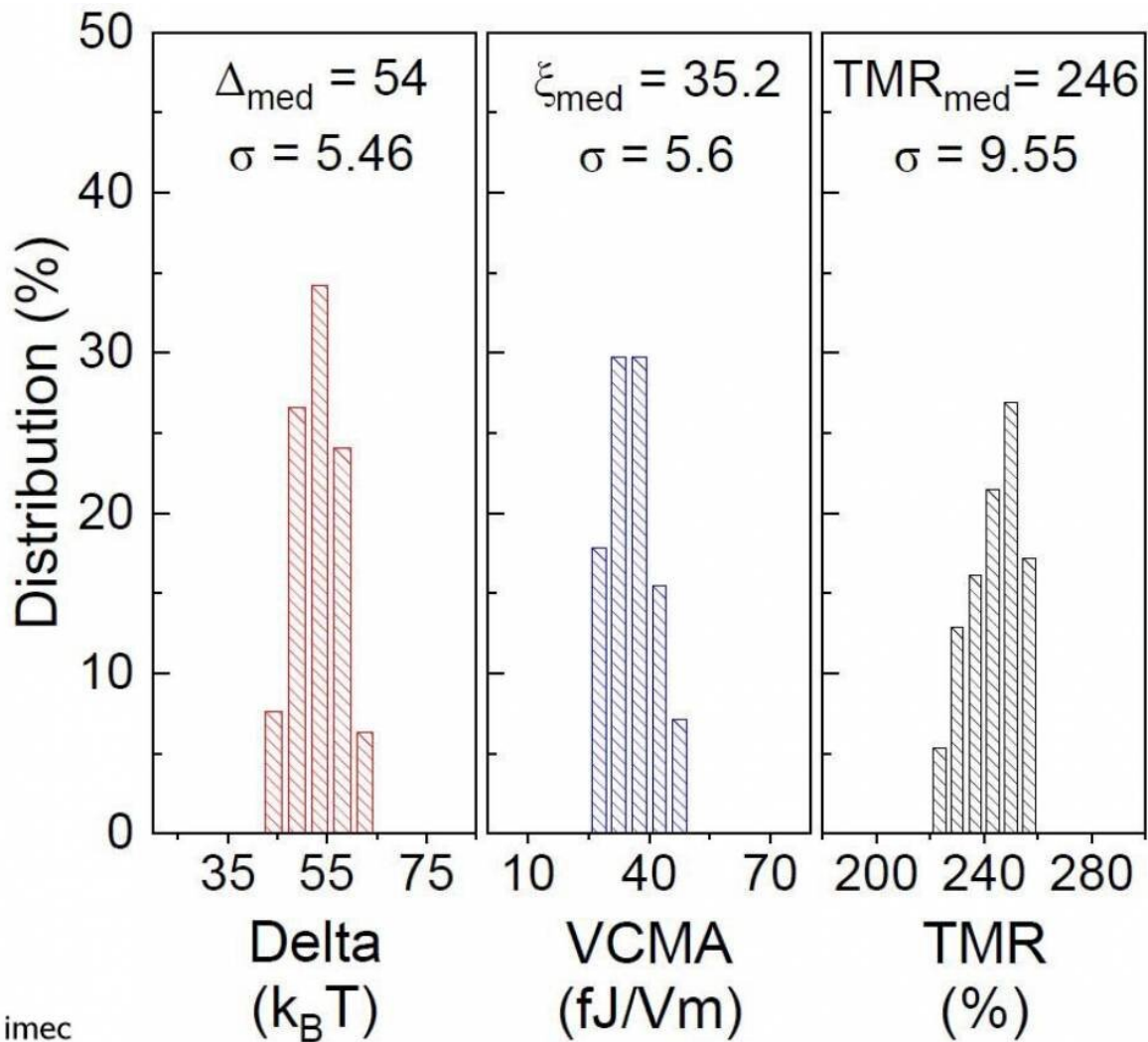
(Bz,eff) in the VCMA stack design.

Figure 2: Figures of merit for the VCMA MRAM device. The graph shows distributions of the fundamental parameters for the baseline devices, with Δ = 54, VCMA coefficient = 35.2fJ/Vm and TMR = 246% in median. Credit: IMEC

As a second improvement, imec embedded a magnetic hardmask on top of the magnetic tunnel junction. This eliminates the need for an external

magnetic field during VCMA switching, improving the device's manufacturability without degrading its performance.

The devices were fabricated using imec's 300mm state-of-the-art technology infrastructure, proving their compatibility with CMOS technology. Reliable 1.1GHz (or ns-scale speed) external-magnetic-field-free VCMA switching was demonstrated with only 20fJ write energy. A high tunnel magnetoresistance of 246% and an endurance of more than 10^{10} have been achieved.

Gouri Sankar Kar, program director at imec, says, "These improvements bring VCMA MRAM performance beyond STT-MRAM operation, making the devices ideal candidates for high-performance, low-power and high-density memory application—serving advanced computational needs or analog compute-in-memory applications."

  More information: Further information on imec can be found at www.imec-int.com

Provided by IMEC