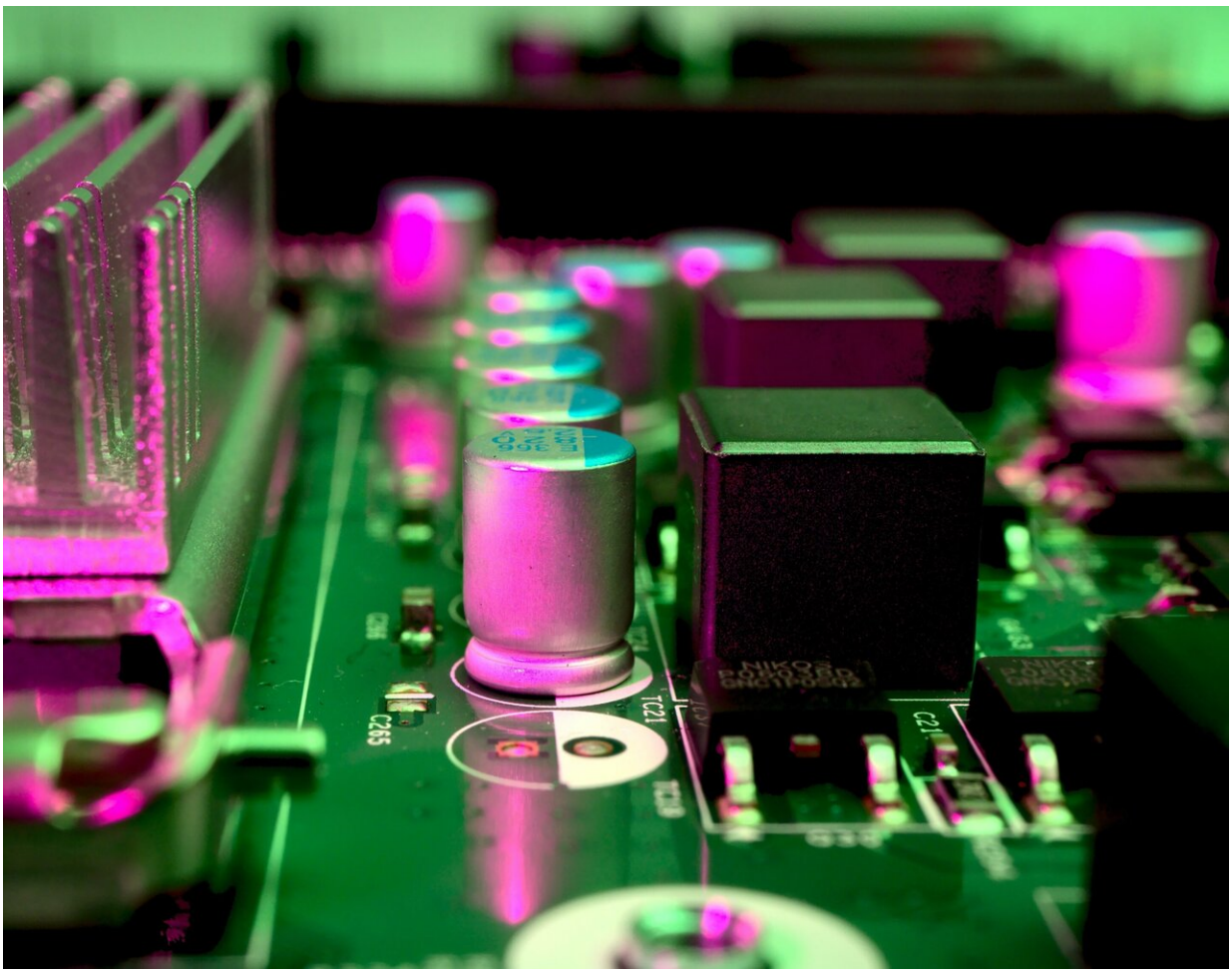
Computer engineers design research platform for mixing processor cores to boost performance

June 19 2020, by Adam Hadhazy



Credit: Unsplash/CC0 Public Domain

Computers are renowned for flexibility, running everything from game consoles to stock exchanges. But at the level of computation, most computers rely on arrays of identical processors called cores. Now, a team at Princeton University has built a hardware platform that allows different kinds of computer cores to fit together, allowing designers to customize systems in new ways.

The goal is to create new systems that parcel out tasks among specialized cores, increasing efficiency and speed.

On top of multi-core collaboration, even more gains are achievable when cores needn't all rely on the same basic programming code that tells a core how to handle its processing jobs. Designers call this basic code an Instruction Set Architecture (ISA). Well-established ISAs include Intel x86, commonly found in laptops, ARM in smartphones, and POWER in IBM mainframes. Besides mixing together cores specialized for different ISAs, researchers are also interested in developing hybrid ISAs to underpin new processor designs, exploiting the potential of new, cutting-edge, open-source ISAs like RISC-V ISA.

What the computer research field has lacked, however, is an experimental hardware platform that allows designers to try out heterogeneous core and ISA arrangements. The Princeton platform, called Bring Your Own Core (BYOC), is open-source, granting anyone who wants to take advantage of its capabilities the opportunity to do so.

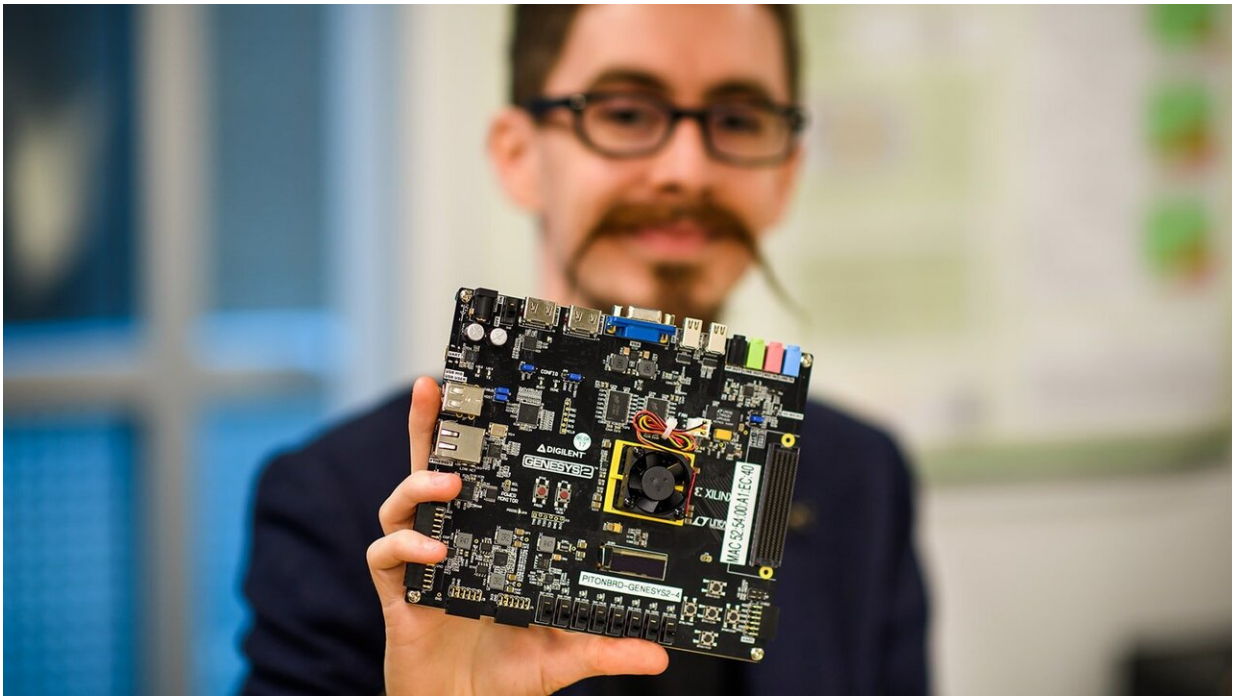
"With Bring Your Own Core, it's right there in the name," said Jonathan Balkind, a graduate student in computer science at Princeton. "Researchers can connect their cores into our modifiable hardware framework, which readily supports multiple ISAs and can scale to handle as many as half a billion cores."

The hope is that this avenue of research will eke out fresh gains now that

Moore's Law—the 1965 observation that computer chips' performance doubles every two years—has lost sway after decades of steady progress.

"In the post-Moore fight to get still more computing performance," said Balkind, "heterogeneous ISA is a key weapon to have in the arsenal, and BYOC will give researchers a way to really develop these capabilities."

Balkind is lead author of a paper presented at The International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2020 that was to be held in Lausanne, Switzerland the week of March 16, but was instead held virtually due to concerns over COVID-19.



Researchers have built a platform allowing computer designers to customize systems in new ways. Credit: Sameer A. Khan/Fotobuddy

"We're really excited about the potential for BYOC, not only for our own heterogeneous ISA research motivations but for the broader research community," said David Wentzlaff, an associate professor of electrical engineering and associated faculty in the Department of Computer Science at Princeton University who advises Balkind and other Princeton co-authors of the paper.

These co-authors include graduate students Grigory Chirkov, Fei Gao, Alexey Lavrov and Ang Li. Former Princeton students Katie Lim, now at the University of Washington, Yaosheng Fu, now at NVIDIA, and Tri Nguyen, now at Harvard University, are also co-authors, as were Luca Benini, Michael Shaffner and Florian Zaruba, researchers at ETH Zürich in Switzerland, and Kunal Gulati of BITS Pilani in India.

BYOC functions on two basic levels. The first is a detailed simulation of hardware, down to where every wire and component in a computer chip would logically go. The second is an emulation of the chip architecture, run on reprogrammable hardware. The emulation approximates how a real computer chip utilizing select cores and ISAs would look and function.

As described in the new paper, the Princeton research team has succeeded in hooking up 10 cores to a BYOC platform that accommodates four separate ISAs, though as Balkind pointed out, that is merely a starting point.

Just one of the many applications for BYOC-enabled research is the design of new computer systems mixing legacy cores with cutting-edge cores, which can help with use cases where legacy cores are needed. .

Smartphones are another application where innovative core and ISA deployment could boost the user experience. A simple depiction of how BYOC could help is by developing novel arrangements that divvy up

tasks amongst big, energy-hogging cores when performance is the goal, or smaller, thrifty cores when energy efficiency is desired. Security is also a consideration, with some ISAs supporting unique security-enhancing features.

After validation with BYOC, researchers might then choose to have their designed chip made into a fully realized, physical form, fabricated by computer chip making companies. Balkind and colleagues plan to do so later this year, culminating nearly three years of efforts into developing and leveraging BYOC.

"I'm very satisfied with what we've accomplished with Bring Your Own Core and I look forward to other researchers working with it," said Balkind. "I'm also very pleased that we made BYOC open source. Given the resources we are fortunate to have here at Princeton and the funding we have received from public sources, it is important that our platform also benefits the general research community."

More information: Jonathan Balkind et al. BYOC, *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems* (2020). DOI: 10.1145/3373376.3378479

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