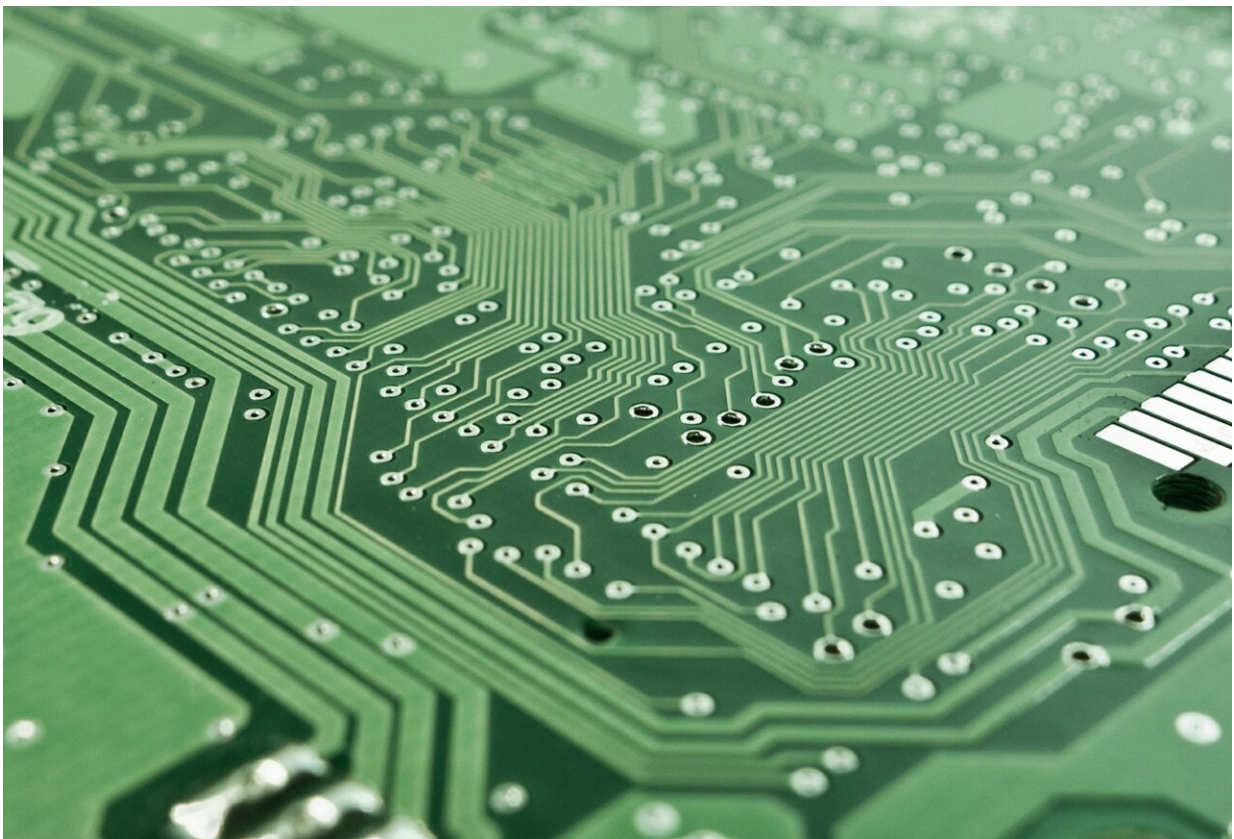


Engineers quintuple the efficiency of moving data bits in silicon chips for artificial intelligence applications

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The Green IC research team at the National University of Singapore has developed an innovative technique that allows the transfer of bits (the

basic unit of information in computing) across a silicon chip up to five times more efficiently than standard setups.

This breakthrough is advantageous for applications such as machine learning, where many processing cores called "neurons" are constantly exchanging data, requiring ever-increasing levels of power. Such power consumption must be significantly reduced to allow for extended battery life in next-generation smartphones, smart watches, and other mobile devices that require higher computing performance.

Led by Professor Massimo Alioto from NUS Electrical and Computer Engineering, the invention by the NUS team enables a new generation of intelligent high-performance systems, where many more neurons can exchange data, while fitting the limited power budget of battery-powered systems. Such higher-performance machine learning processing translates into new capabilities, from augmented reality, to continuous monitoring of wearable electronics, speech recognition, automatic video quality enhancement, secure user authentication, and more.

"Artificial intelligence and other popular computationally-intensive applications require an increasing number of neurons to deliver the necessary performance. As a result, the power consumption jumps quadratically with the number of cores. Our research demonstrates that the rising power consumption of these setups can be now tamed, allowing a sustainable increase in the number of cores for future generations of intelligent chips," explained Prof Alioto.

"Our [silicon chip](#) demonstration sets a new standard for power efficiency, without modifying the building blocks, such as transmitters and receivers, that are typically used in these setups, allowing its easy adoption in existing designs. Given that power, performance and cost are all fundamental drivers of [artificial intelligence](#) applications, our invention simplifies the integration of next-generation intelligent

systems," he said.

A network on a chip with a dynamic energy-quality trade-off

Today's silicon systems generally adopt a "network on a chip" to implement the communication features between the different processing elements on the same chip. In the case of large-scale designs, networks-on-chip reduce the complexity involved in designing the wires and also provides a streamlined structure capable of improved performance, power efficiency and reliability.



Dr Viveka Konandur (left) and Prof Massimo Alioto (right) from the Green IC group testing the network-on-chip in a machine learning application. Credit: National University of Singapore

The invention from the NUS researchers is a network-on-chip that achieves an uncommonly favorable energy-quality trade-off, substantially reducing power consumption at an insignificant loss in quality. This property permits the amplitude (voltage swing) of the transmitted signal to be dynamically adjusted, setting it to conventional values for maximum accuracy in mission-critical tasks. Lower voltage swings reduce the power consumption at minimal accuracy reduction.

As an example, this dynamic energy-quality scaling achieves prolonged [battery life](#) by allowing an imperceptible video quality degradation, when full quality is not necessary. This is the case for most practical uses of smartphones, when the quality of ambient lighting is less than optimal, when the user is not paying full attention to the content, or when the battery level is low. Such operating conditions are easily identified by light sensors, camera sensors, and battery monitors, and are used to reduce power when allowed.

The network-on-chip demonstrated by the Green IC group can also run at three times lower power for the same quality, compared to state-of-the-art approximate networks using a lower number of bits to save power.

"The proposed network-on-chip is part of a broad research investigation of energy-quality scalable systems, which have been pioneered by our group and demonstrated in several chips for vision, auditive intelligence, memory, processing, and sensor interfaces, among others," he said.

"Energy-quality scalable networks-on-chip were the missing link in fully-scalable systems that can run at full accuracy if required, or reduce consumption down to best-in-class when full accuracy is not required. In our approach, most significant bits are dynamically routed to network wires that happen to be affected by usual levels of variations, while steering least significant bits to the wires that experience more variations."

Next steps

The development of the network-on-chip with five times lower power consumption is a key step towards the demonstration of a full 'computer vision system.' Computer vision is the field of computer science that focuses on replicating the human vision system, enabling computers to identify and process objects in images and videos in the same way that humans do.

The NUS invention paves the way for a computer vision system where all components are energy-quality scalable, and are simultaneously adjusted to operate at the lowest power whilst maintaining an acceptable level of accuracy. The underlying research aims to demonstrate a new breed of low-power smart cameras that could operate almost perpetually under the tight [power](#) budget extracted from the environment such as via a centimeter-sized solar cell, eliminating the conventional need for wires and cables.

Provided by National University of Singapore

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