Reliable, high-speed MTJ technology for 1X nm STT-MRAM and NV-logic has wide applications

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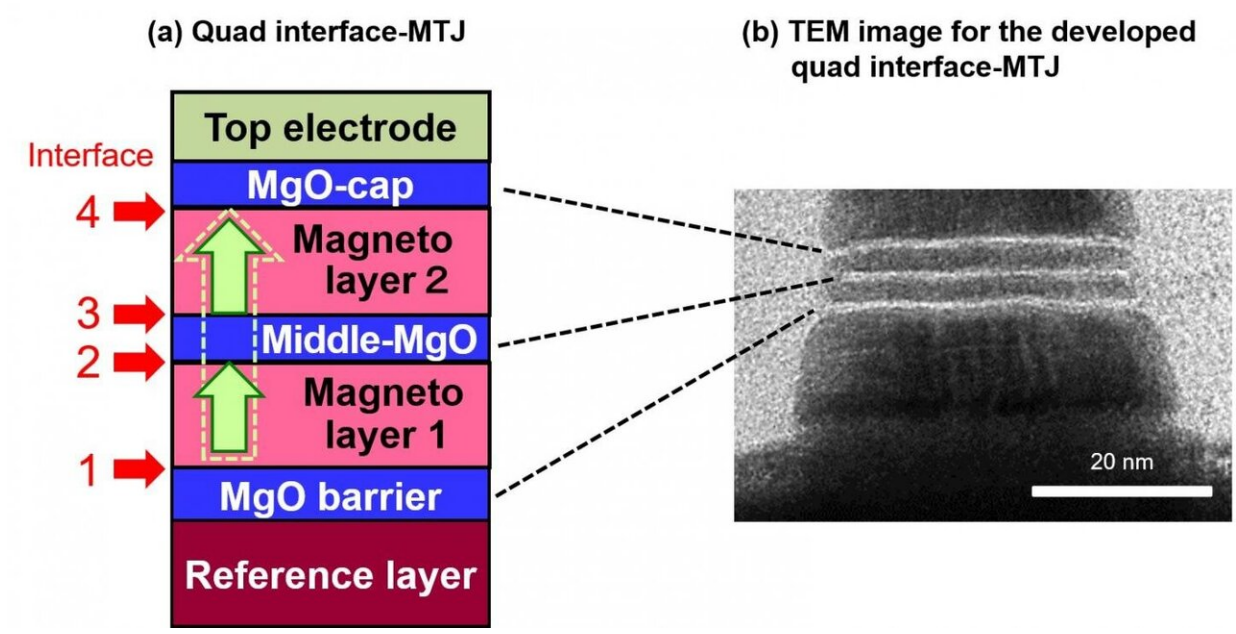

(a) Schematic and (b) TEM image of the developed quad -interface MTJ structure in this study. Credit: Tohoku University

Professor Tetsuo Endoh, leading a group of researchers at Tohoku University, has announced the development of an MTJ (Magnetic Tunnel Junction) with 10 ns high-speed write operation, sufficient endurance ($>10^{11}$), and with highly reliable data retention over 10 years at 1X nm size. Realizing a 1X nm STT-MRAM (Spin Transfer Torque-

Magnetoresistive Random Access Memory) and NV(Non-Volatile)-Logic has wide application to a variety of fields.

Because STT-MRAM and NV-Logic with MTJ/CMOS hybrid technology offer low power consumption, they are essential constituents in semiconductor memory and logic such as processors. To put spintronics technology to practical use, higher speed write operation, lower power consumption, and greater endurance are required. Additional needs include data retention exceeding 10 years, a higher operation temperature, and excellent scalability. However, there has been a significant problem with data retention, which is often achieved at the expense of operational performance such as write speed, write power, endurance and so on. This problem has seriously limited the application field of STT-MRAM and NV-Logic.

For the application of 1X nm node STT-MRAM and NV-Logic to a wide variety of fields, the research team developed a new MTJ stack design technology and highly reliable fabrication technology for Quad interface type iPMA-MTJ (Quad-MTJ).

Using the new technologies—first proposed and demonstrated by the same team last year—resulted in a successful fabrication of advanced Quad-MTJ. The research team has now been able to demonstrate that the current write density of Quad-MTJ can be reduced by over 20% at a 10ns high speed write operation in comparison with the conventional Double-MTJ—even though the thermal stability factor of Quad-MTJ is 2 times larger than Double-MTJ. In other words, the data retention of Quad-MTJ can be maintained for a period exceeding 10 years and at a higher operating temperature than Double-MTJ. Moreover, Quad-MTJ achieved satisfactory endurance levels (over 10^{11}), performing better than Double-MTJ, even though the data retention of Quad-MTJ is superior to that of Double-MTJ.

The research team states that the advanced Quad-MTJ overcomes the serious issue of conventional Double-MTJ in several ways: the dilemma between data retention and many kinds of operation performance such as write speed, write power, endurance and so on.

As a result, these developed Quad-MTJ technologies, 1X nm STT-MRAM and NV-Logic with MTJ/CMOS hybrid technology will open a new spintronics base LSI suitable for wide applications including low-end fields (such as IoT systems and sensor network systems); high-end fields (such as AI systems and image processing systems); and the field of tolerance property for application in tougher environments (such as automobile parts, production facility systems and so on).

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Results will be presented at this year's Symposia on VLSI Technology and Circuits as a virtual conference from June 14-19, 2020. In addition, the study was included in the "Technical Highlights from the 2020 Symposia on VLSI Technology & Circuits."

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