New DDR5 SDRAM standard sees performance boost, dual-channel DIMM

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They were two years behind schedule but the industry group overseeing

memory technology development and standardization has finally announced the officials specs for the new DDR5 SDRAM standard.

The JEDEC Solid State Technology Association said I'm a report issued Tuesday the new memory specifications will provide developers with twice the performance power and lower power consumption.

Among the key improvements will be a quadrupling of maximum die density, up to 64 gigabytes from 16 gigabytes under the old standard. Each DIMM can handle two 32-bit memory channels instead of only a single 64-bit channel. Since each bank operates independently of each other, the burst length can be doubled and greater efficiency can be achieved. That means, for instance, DDR5 SDRAM can perform two 64-byte operations in the same time it takes DDR4 SDRAM to perform just one operation.

Also improving power consumption demands will be an integrated voltage regulator. Such regulators previously were situated on motherboards. The new spec allows manufacturers to incorporate as many regulators as necessary to accommodate the number of DIMMs on end systems. This should reduce the cost and simplify the design of motherboards. With each DIMM providing its own voltage regulation, JEDEC refers to this approach as "pay as you go."

Yet to be determined is how much improvement in power efficiency will be achieved with the slightly lower power consumption, 1.1 volts, compared with 1.2 volts for DDR4. The DDR4 specs had improved upon earlier numbers by 0.3 volts, 1.2 volts compared with 1.5 volts for DDR3.

As far as maximum data rates, DDR5 will handle 6.4 Gbps, doubling the DDR4 standard, although the first modules to reach market will be capped at 4.8 Gbps.

"With the publication of JEDEC's DDR5 standard, we are entering a new era of DDR performance and capabilities," said Intel's Carolyn Duran, a vice president of the Data Platforms Group. "DDR5 marks a great leap forward in memory capability, for the first time delivering a 50 percent bandwidth jump at the onset of a new technology to meet the demands of AI and high performance compute."

The first consumer products with DDR5 specs are expected to roll off assembly lines some time in 2021.

JEDEC, composed of representatives from 300 member companies, said it recognizes the growing performance demands of intensive cloud and enterprise data center applications.

The efforts of the group "have resulted in a standard that addresses all aspects of the industry, including system requirements, manufacturing processes, circuit design, and simulation tools and test, greatly enhancing developers' abilities to innovate and advance a wide range of technological applications," said Desi Rhoden, chairman of the JC-42 Memory Committee and executive vice president of Montage Technology.

"With several new performance, reliability and power saving modes implemented in its design, DDR5 is ready to support and enable next-generation technologies," he said.

Frank Ross, senior member of Technical Staff at Micron and a member of the JEDEC Board of Directors, said, "The DDR5 standard offers the industry a critical advancement in main memory performance to enable the next-generation of computing required to turn data into insight across cloud, enterprise, networking, high-performance computing and artificial intelligence applications."