A new strategy to implement XY entangling gates in superconducting qubit architectures
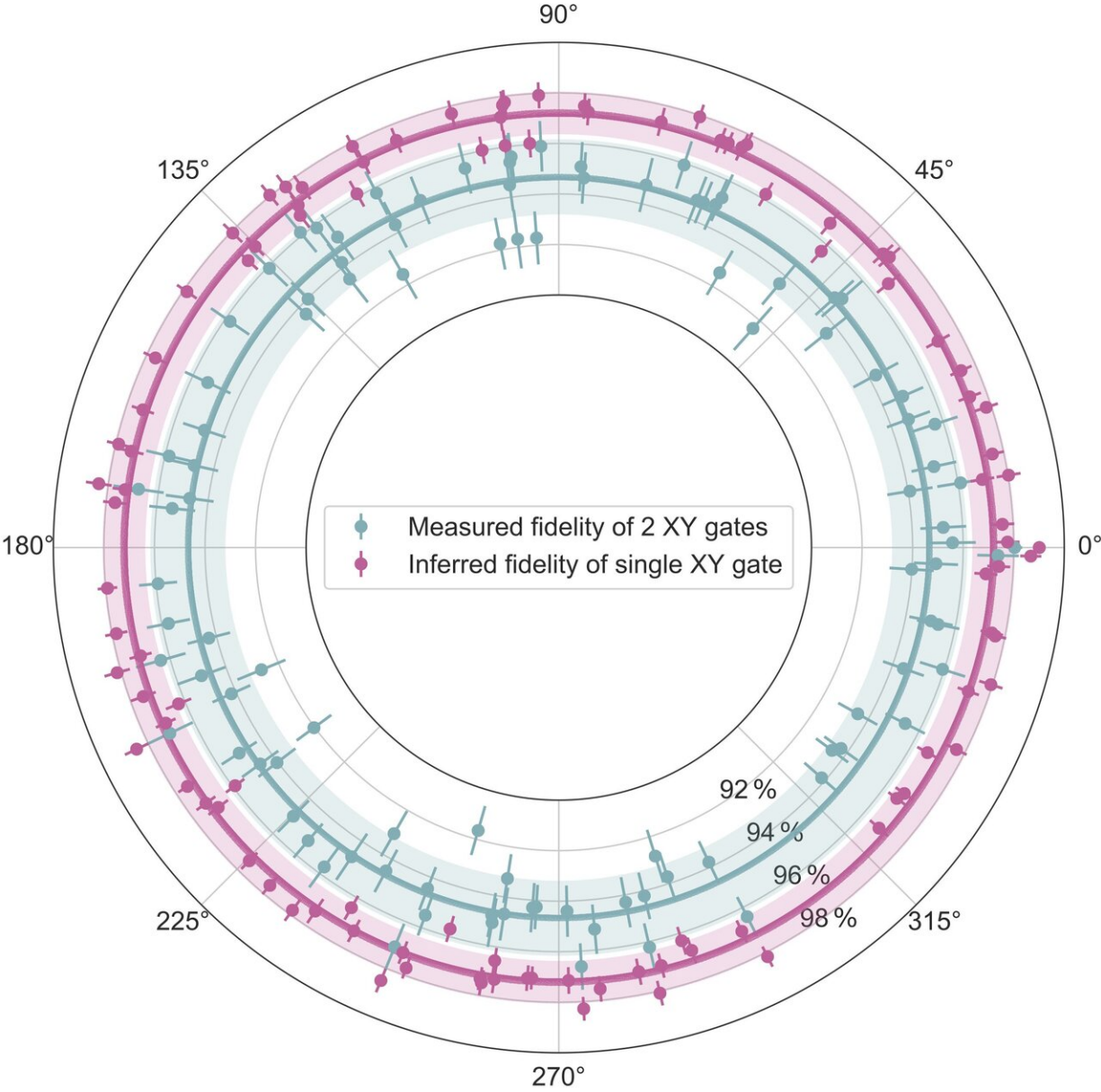
January 7 2021, by Ingrid Fadelli

Fidelity of XY(θ) gates as a function of the angle θ (magenta). Credit: Abrams et al.

Over the past decade or so, research teams worldwide have been trying to develop devices and hardware components for quantum information processing. The performance of most of these emerging devices depends in great part on optimized circuit implementations that can minimize the depth of a circuit.

A possible way to achieve this is to use more expensive and sophisticated native gates. XY two-qubit gates have proved to be particularly promising for reducing the depth of generic circuits, while also improving the performance of quantum processors on specific problems.

Researchers at Rigetti Computing recently demonstrated the potential of using XY entangling gates to improve the performance of a tansmon-based superconducting qubit architecture. Their approach, outlined in a paper published in *Nature Electronics*, requires only the use of a single calibrated pulse.

"In the effort to improve the performance of quantum processors, it is advantageous to offer expressive sets of native gates in order to reduce the compilation overhead from algorithms to hardware," Dr. Nicolas Didier, one of the researchers who carried out the study, told Tech Xplore. "For variational quantum algorithms in particular, it helps to have continuous entangling gate families. In this work, we developed an efficient implementation of the XY family on transmon qubits."

Didier and his colleagues devised a new strategy for implementing entangling gates in a transmon-based superconducting qubit architecture. This method allowed them to control the phase of the qubit-qubit

interaction in the architecture by applying a flux pulse.

"To generate the full XY family, we simply split the iSWAP gate into two $\sqrt{i}$SWAP gates and change the phase in between," Didier said. "The full family is obtained by calibrating only the pulse for $\sqrt{i}$SWAP, it provides an efficient method to regularly retune our deployed quantum processors. (iSWAP = XY(π) and $\sqrt{i}$SWAP = XY($\pi/2$), square root of iSWAP)."

The new strategy enabled the implementation of XY entangling gates in the superconducting system to which they applied it, with high levels of fidelity. Didier and his colleagues also demonstrated that their method can be used to implement quantum approximate optimization algorithms, reducing circuit depths by approximately 30% compared to strategies based on the sole use of CZ gates.

"We generated the family of XY gates with fidelities between 96 and 99%," Didier said. "These gates are operated at dynamical sweet spots to mitigate dephasing due to slow flux noise. We also illustrated the advantage of expressive sets of native gates on the QAOA algorithm, showing that combining iSWAP and CZ provides a reduction of 30% in gate depth."

The strategy presented by this team of researchers could ultimately inform the development of better performing and more efficient [quantum information](#) processors. In their paper, the researchers show that their gate decomposition strategy can be extended to other types of native gates, which could enable further reductions in circuit depth.

"Our approach can be extended to the CPHASE family of two-qubit gates, and the CCPHASE family of three-qubit gates by calibrating only two pulses, with a 2-6x depth reduction compared to previous implementations," Didier said. "Users of Rigetti [quantum processors](#) can

try to reduce the compiled gate depth themselves using Quil-T, our pulse-level control interface."

More information: Implementation of XY entangling gates with a single calibrated pulse. *Nature Electronics*(2020). [DOI: 10.1038/s41928-020-00498-1](#)

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