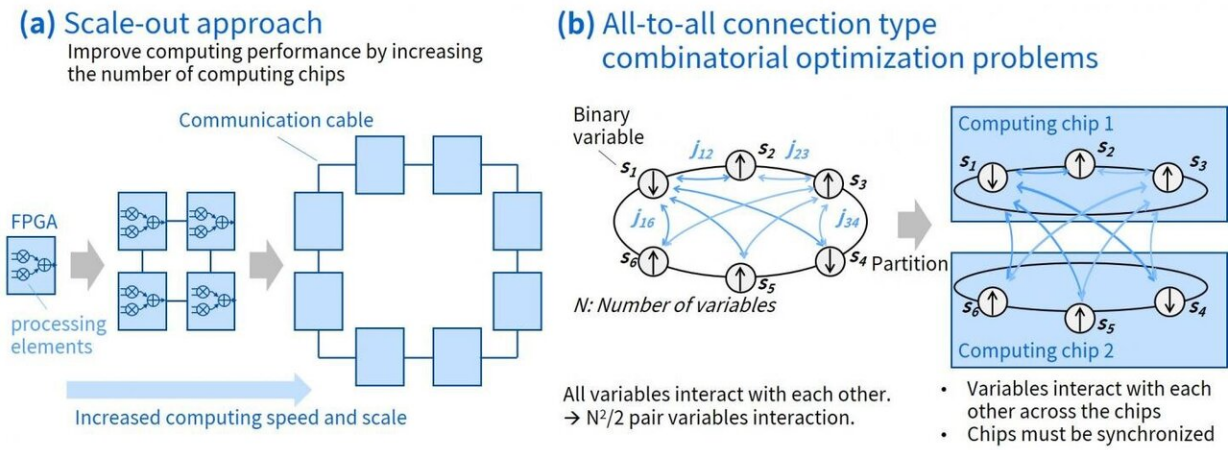
Cutting-edge scale-out technology from will take fintech and logistics to new level

March 12 2021



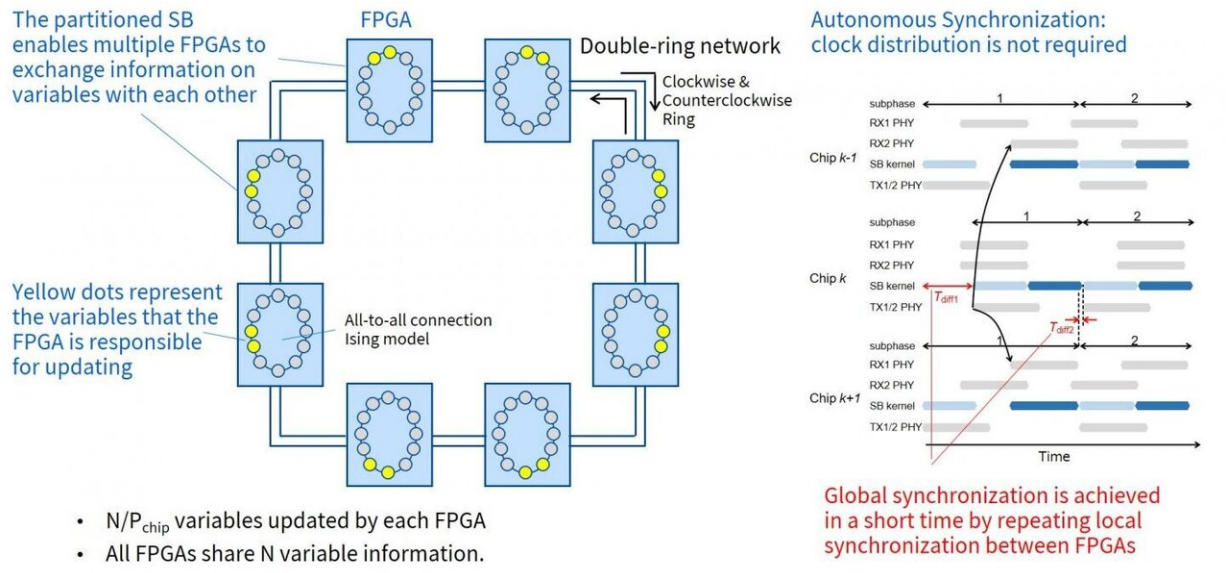
(a) Scale-out approach: improve computing performance by increasing the numbers of computing chips; (b) All-to-all connection type combinatorial optimization problems: all variables interact with each other. Credit: Toshiba Corporation

Toshiba Corporation, the industry leader in solutions for large-scale optimization problems, today announced a scale-out technology that minimizes hardware limitations, an evolution of its optimization computer, the Simulation Bifurcation Machine (SBM), that supports continued increases in computing speed and scale. Toshiba expects the new SBM to be a game changer for real-world problems that require large-scale, high-speed and low-latency, such as simultaneous financial

transactions involving large numbers of stock, and complex control of multiple robots. The research results were published in *Nature Electronics* on March 1.

Speed and scale are keys to success in industrial sectors as different as finance, logistics, and communications, all of which have to deal with large numbers and make complex decisions in the shortest time possible. Aiming to bring higher efficiencies to these and other businesses, Toshiba has addressed combinatorial optimization problems by developing high-speed, high-accuracy algorithms and corresponding practical computer solutions. The company recently announced a second generation of its simulated bifurcation algorithms, implemented on classical computers via a single field programmable gate array (FPGA), that surpasses quantum computers in obtaining optimal solutions for various combinatorial optimization problems at high speed.

Toshiba continues to pursue better performance of the SBM by installing more FPGAs in the computer, an approach called scale-out in computer architecture, and has successfully demonstrated the world's first simultaneous scale-out of computing speed and problem size for all-to-all connection type combinatorial optimization problems. At the heart of the technology is a partitioned version of the simulated bifurcation algorithm that enables multiple FPGAs to exchange information on variables with each other, and that triggers an autonomous synchronization mechanism in minimizing the communications overhead to an extent that does not affect overall performance.



Toshiba's new scale-out technology: A new multi-chip architecture featuring a partitioned version of the simulated bifurcation algorithm (partitioned SB) and an autonomous synchronization mechanism. Credit: Toshiba Corporation

Trials has shown that an SBM with a cluster of eight FPGA achieves computational throughput 5.4 times higher than an SBM with single FPGA, and solve problems 16 times larger; and simulation results with a 64 FPGA SBM have demonstrated that the relationship between the computing speed and number of FPGA is exactly linear, indicating that the technology can continue to increase the scale-out with the same effect.

The 8 FPGA SBM also obtains solutions 828 times faster than an implementation of simulated annealing (SA), a widely used optimization technique, demonstrating that the SBM makes much more efficient use of computational resources than the SA.

Figure 3

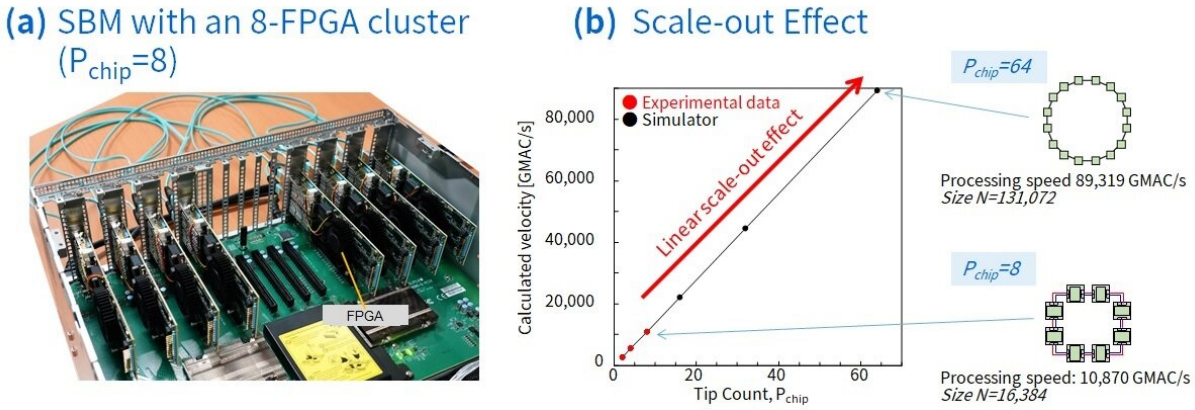
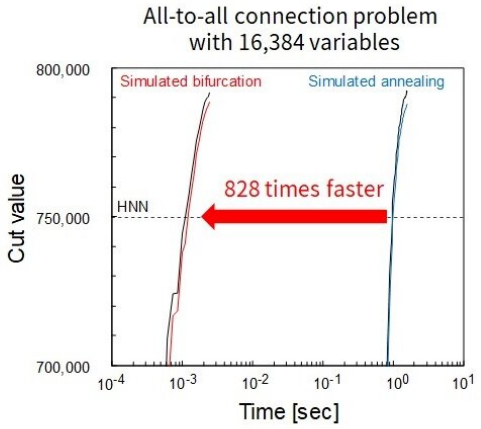


Figure 4



(a) SBM with an 8-FPGA cluster. (b) scale-out effect / Figure 4: Comparison of the computing time on 8 FPGA SBM and SA. Credit: Toshiba Corporation

Commenting on the application of the technology, Kosuke Tatsumura, Chief Research Scientist at Toshiba Corporation's Corporate Research & Development Center, said: "Fast computing speed, large computing scale, and low latency to provide solutions are the critical values the new SBM can offer to business. For example, we expect the financial

industry can benefit if they can trade more stocks simultaneously, and robots in the logistic industry will perform better with zero-time-lag computation. We hope the new technology will take fintech and logistic to a new level."

More information: Kosuke Tatsumura et al, Scaling out Ising machines using a multi-chip architecture for simulated bifurcation, *Nature Electronics* (2021). DOI: 10.1038/s41928-021-00546-4

Provided by Toshiba Corporation