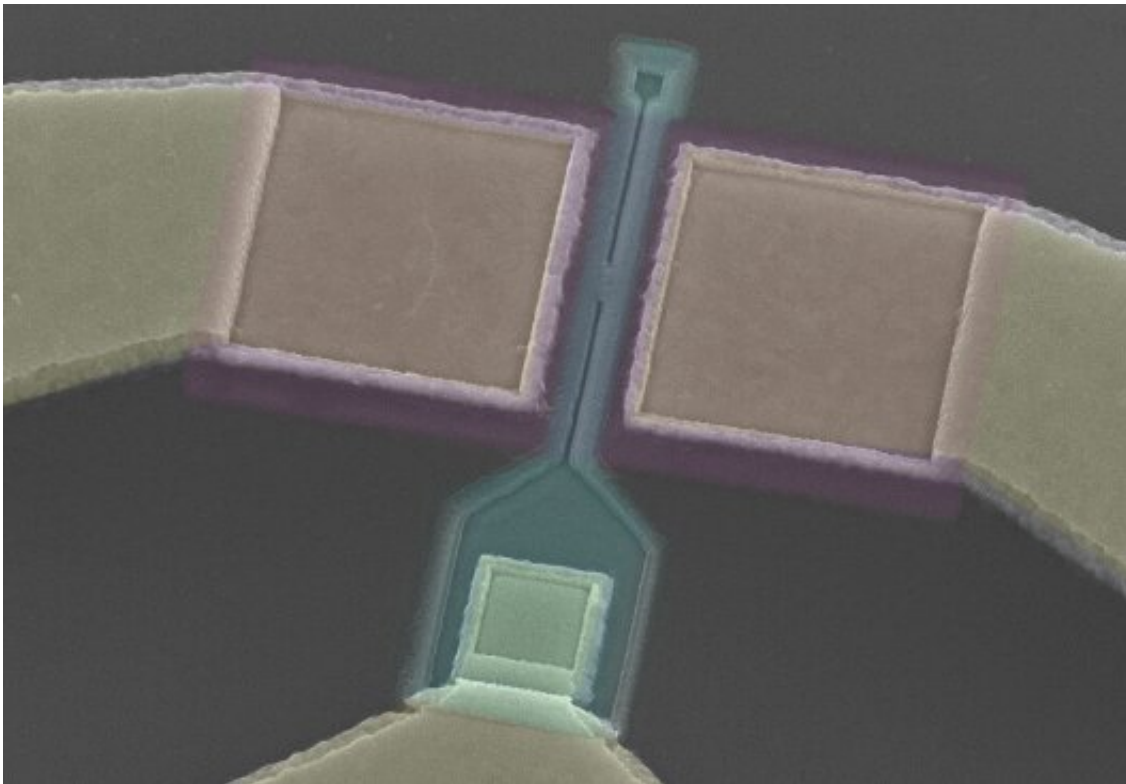


Researchers create a hybrid technology that combines III-V tunnel FETs and MOSFETs

March 10 2021, by Ingrid Fadelli



False-colored scanning electron microscopy (SEM) image of a Tunnel FET top-view, after metallization. Credit: Convertino et al.

Over the past few decades, the incredible progress made in the electronics industry has been partially driven by innovations at the single-transistor level. A transistor is a semiconducting device that can conduct, insulate and amplify electric current inside electronic circuits. Building

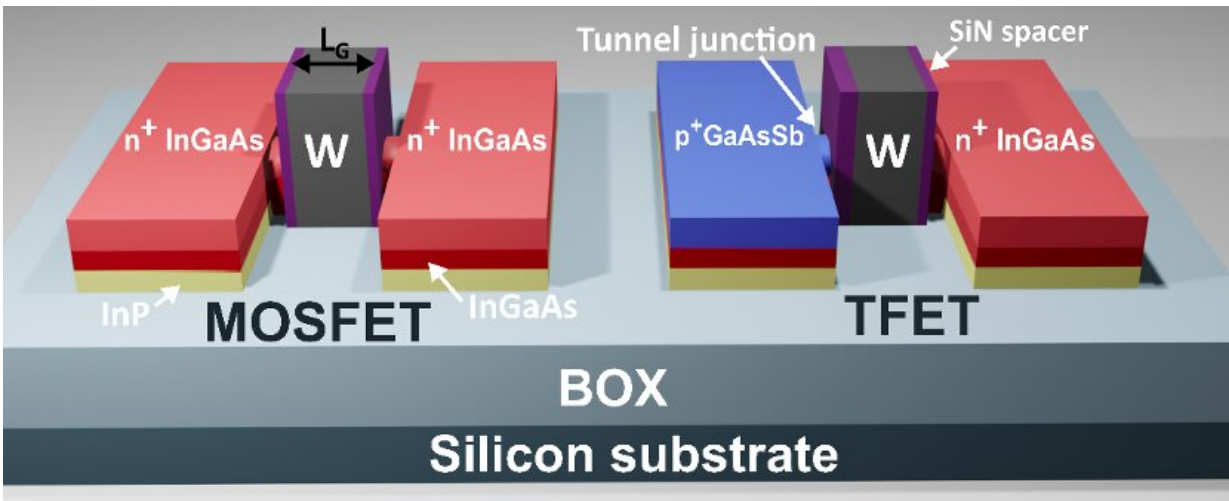
faster and smaller transistors has been a primary goal for the semiconductor industry over the past few years.

Metal-oxide-semiconductor field-effect [transistors](#) (MOSFETs) are the most conventional and widely used type of transistors. One of their major limitations is their high power inefficiency, which is due to their inability to reduce the voltage supply while simultaneously limiting the off-state leakage current.

A novel and alternative type of [device](#) called a tunnel field-effect transistor (TFET) can overcome this limitation by leveraging quantum mechanical tunneling instead of thermionic emission. TFETs, particularly those with a III-V heterostructure, require less than 60 mV of gate voltage swing to induce a variation of one order of magnitude in the drain current at ambient temperatures. Despite their [lower power consumption](#), TFETs have not yet achieved the remarkable speed and energy efficiency of MOSFETs at higher drive voltages.

Researchers at IBM Research Europe and at École Polytechnique Fédérale de Lausanne (EPFL) have recently developed the first silicon-based hybrid device that combines III-V tunnel FETs and conventional MOSFETs. The technology they developed, presented in a paper published in *Nature Electronics*, combines the advantages of the two different transistor designs.

"We demonstrated the first hybrid technology platform combining III-V tunnel FETs and MOSFETs with a scalable process and suitable for large-scale semiconductor manufacturing," Clarissa Convertino, one of the researchers who carried out the study, told TechXplore. "Such low-power technology platform paves the way to future energy efficient electronics, with the ultimate goal of reducing the carbon footprint of the ICT industry."



3D schematic representing the developed technology platform. The MOSFET (on the left) differs from the Tunnel FET (on the right) only in the use of different materials in the transistor source region. Credit: Convertino et al.

The new platform developed by Convertino and her colleagues exploits the synergies between tunnel FETs and MOSFETs, as it allows users to implement hybrid logic blocks tailored to the unique specifics of each type of device. In initial evaluations, the scaled III-V hybrid TFET-MOSFET device achieved a minimum subthreshold slope of 42 mV dec^{-1} for TFET devices and 62 mV dec^{-1} for MOSFET devices.

"Tunnel FETs provide lower leakage and good performance at low voltages levels, while MOSFETs are faster (at the same dimension and bias) and provide greater current drive," Convertino explained. "The developed fabrication flow is identical for both devices except for a single masking and epitaxy step, opening up for manufacturing of truly hybrid logic blocks. Moreover, our tunnel FETs show record performance at the smallest gate length reported to our best knowledge."

The remarkable performance achieved by the researchers' device is in part due to their introduction of a self-aligned source-replacement step. In their platform, in fact, the position of the GaAsSb source is determined by digital etching, a process that allows them to remove material with a control in the nanometer range.

Convertino and her colleagues were the first to effectively demonstrate the integration of an in-plane heterojunction [tunnel](#) FET in an advanced hybrid platform using replacement metal-gate and spacer technologies. In the future, the technology they created could enable the development of faster and more efficient electronic devices that combine the advantages associated with TFET and MOSFET transistors.

"In our next studies, we will explore the potential of the developed platform and its applications further in different working conditions, such as at cryogenic temperatures, down to the milli-Kelvin regime," Convertino said. "Ultra-low power electronics is particularly interesting for quantum computing applications."

More information: A hybrid III-V tunnel FET and MOSFET technology platform integrated on silicon. *Nature Electronics*(2021). [DOI: 10.1038/s41928-020-00531-3](https://doi.org/10.1038/s41928-020-00531-3).

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