

# New design for isolated power supply chip

May 13 2021

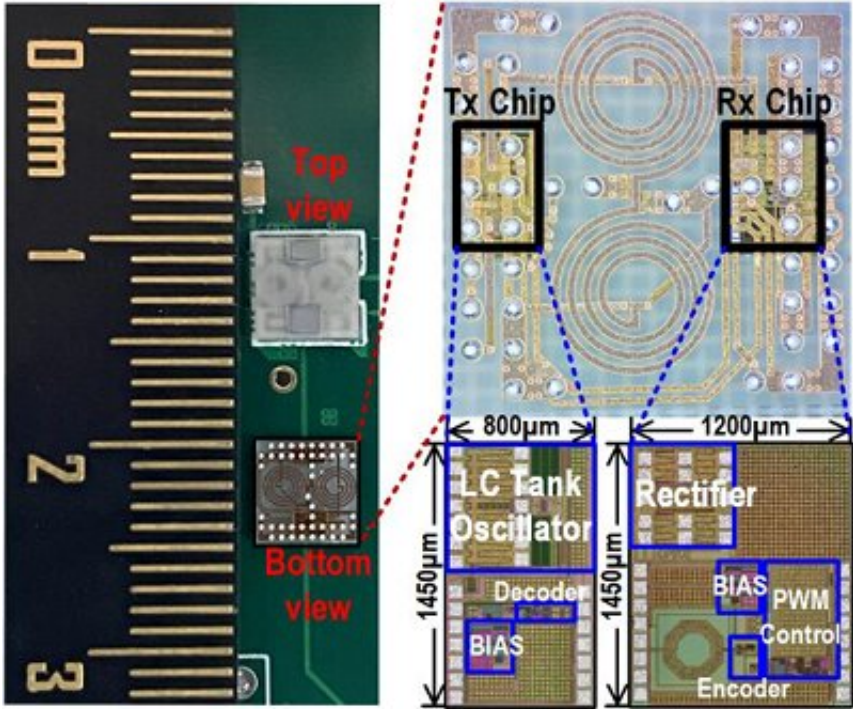


Photo of Isolated power system package and chip. Credit: PAN Dongfang

Recently, a research group led by Prof. Cheng Lin from School of Microelectronics, University of Science and Technology of China (USTC) of the Chinese Academy of Sciences has made achievements in the field of fully integrated isolated power chip design.

The researchers proposed a [chip](#) based on glass fan-out wafer-level package (FOWLP), achieving 46.5% peak transformation efficiency and 50mW/mm<sup>2</sup> power density.

Compared with the traditional isolated power supply chip, this new design interconnects the receiving and transmitting chips through the micro transformer made of the rewiring layer, showing no need of additional transformer chips. In this way, it lowered the need for three or even four chips in the existing chip design, so as to greatly improve the efficiency of isolated [power supply](#).

In addition, the researchers proposed a grid voltage control technology with variable capacitor, which maintains the grid peak voltage in the best safe voltage range even in a wider supply voltage range.

This design improves the conversion efficiency and [power density](#) of the chip effectively, providing a new solution for the design of isolated [power](#) chip in the future.

This work is published at the IEEE International Solid State Circuits Conference (ISSCC), and was selected as the demo demonstration at the meeting.

**More information:** Dongfang Pan et al. 33.5 A 1.25W 46.5%-Peak-Efficiency Transformer-in-Package Isolated DC-DC Converter Using Glass-Based Fan-Out Wafer-Level Packaging Achieving 50mW/mm<sup>2</sup> Power Density, *2021 IEEE International Solid- State Circuits Conference (ISSCC)* (2021). [DOI: 10.1109/ISSCC42613.2021.9365955](https://doi.org/10.1109/ISSCC42613.2021.9365955)

Provided by Chinese Academy of Sciences

Citation: New design for isolated power supply chip (2021, May 13) retrieved 26 April 2024 from <https://techxplore.com/news/2021-05-isolated-power-chip.html>

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