First electrical demonstration of integrated forksheet devices to extend nanosheets beyond 2 nm technology

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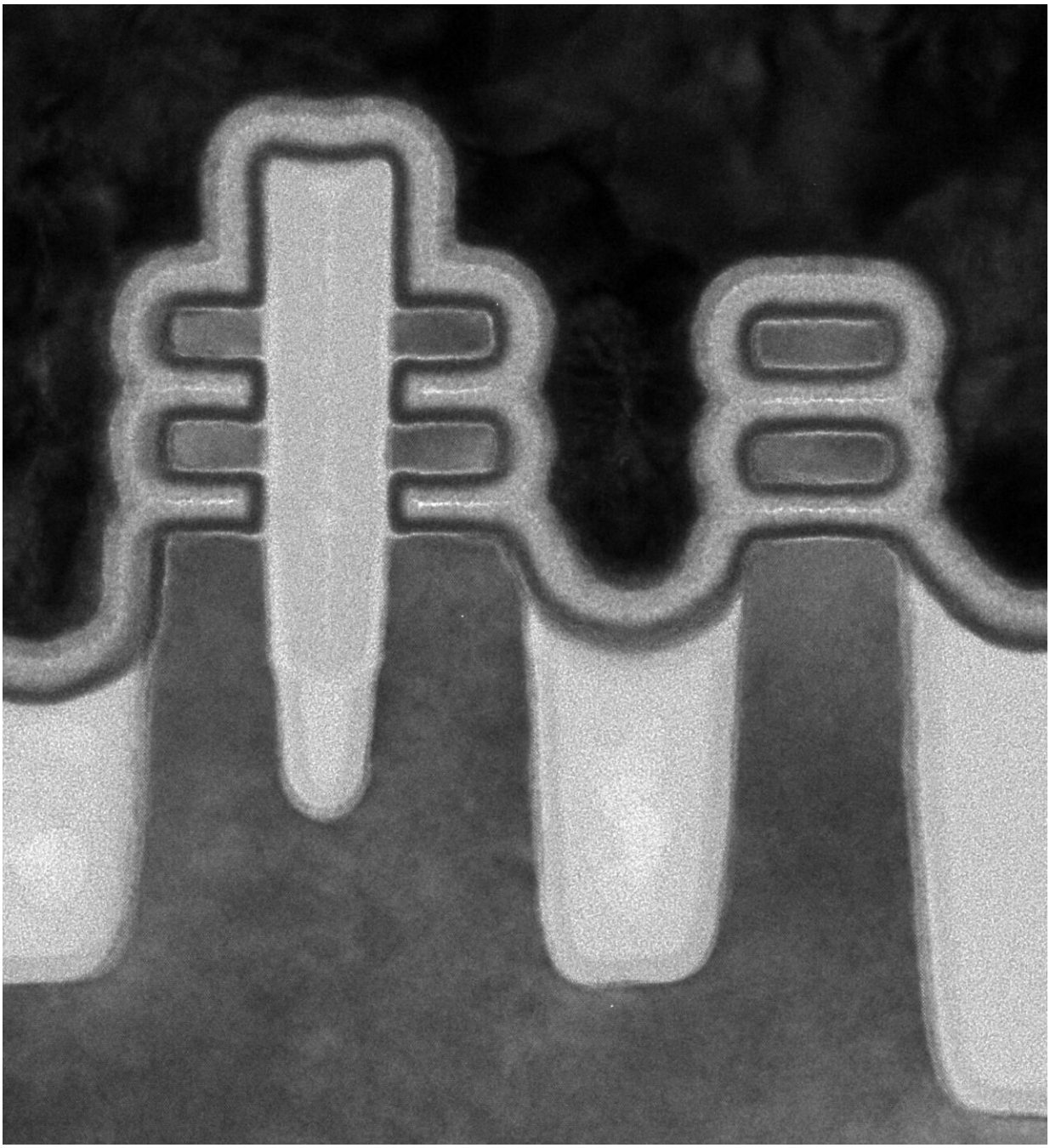

TEM image of co-integrated fork- and nanosheet FETs. For the forksheet n-and pFETs, a dual work function metal gate is integrated at 17nm n-p space. Credit: imec

This week, at the 2021 Symposia on VLSI Technology and Circuits (VLSI 2021), imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, demonstrated for the first time fully functional integrated forksheet field-effect transistors (FETs) with short-channel control (SSSAT=66-68mV/dec) comparable to gate-all-around (GAA) nanosheet devices down to 22-nm gate length. Dual work function metal gates are integrated at 17-nm spacing between n- and pFETs, highlighting the key benefit of forksheet devices for advanced CMOS area scaling.

The forksheet device has recently been proposed by imec as the most promising device architecture to extend the GAA nanosheet device generation with additional scaling and performance beyond 2-nm technology node. Unlike nanosheet devices, the sheets are now controlled by a tri-gate forked structure—realized by introducing a dielectric wall in between the p- and nmOS devices before gate patterning. This wall physically isolates the p-gate trench from the n-gate trench, allowing a much tighter n-to-p spacing than what is possible with either FinFET or nanosheet devices. Technology assessment based on TCAD simulations earlier showed superior area and performance scalability. The performance increase is mainly attributed to a reduced Miller capacitance—resulting from a smaller gate-drain overlap.

Imec presented for the first time an electrical characterization of its forksheet devices that were successfully integrated by using a 300 mm process flow, with gate lengths down to 22 nm. Both n- and pFETs, each with two stacked Si channels, were found to be fully functional. Their short channel control (SSSAT = 66-68mV) was comparable to that of vertically stacked nanosheet devices that were co-integrated on the same wafer. For the forksheet devices, dual work function metal gates were integrated using a replacement metal gate flow at an n-p space as tight as 17 nm (which is about 35% of the spacing in state-of-the-art FinFET technology), highlighting one of the key benefits of the new device

architecture.

"From 2022 onward, it is expected that today's leading-edge FinFET transistors will gradually give way to vertically stacked nanosheet transistors in high-volume manufacturing, as the FinFET fails to provide enough performance at scaled dimensions," explains Naoto Horiguchi, director, CMOS Device Technology at imec. "Process limitations will, however, pose a limit to how close the nanosheet's n and p devices can be brought together, challenging further cell height reduction. The new forksheet device architecture—which is a natural evolution of the GAA nanosheet device—promises to push this limit, allowing track height scaling from 5T to 4.3T while still offering a performance gain. Alternatively, with a forksheet design, the available space can be used to increase the sheet width and as such further enhance the drive current. Our electrical characterization results confirm that the forksheet is the most promising device architecture to extend the logic and SRAM scaling roadmaps beyond 2 nm leveraging the nanosheet integration in a non-disruptive way."

More information: 2021 VLSI Symposia paper - Forksheet FETs for Advanced CMOS Scaling: Forksheet-Nanosheet Co-Integration and Dual Work Function Metal Gates at 17nm N-P Space

Provided by IMEC

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