

# New magnetic tunnel junction quad tech provides endurance and reliable data retention

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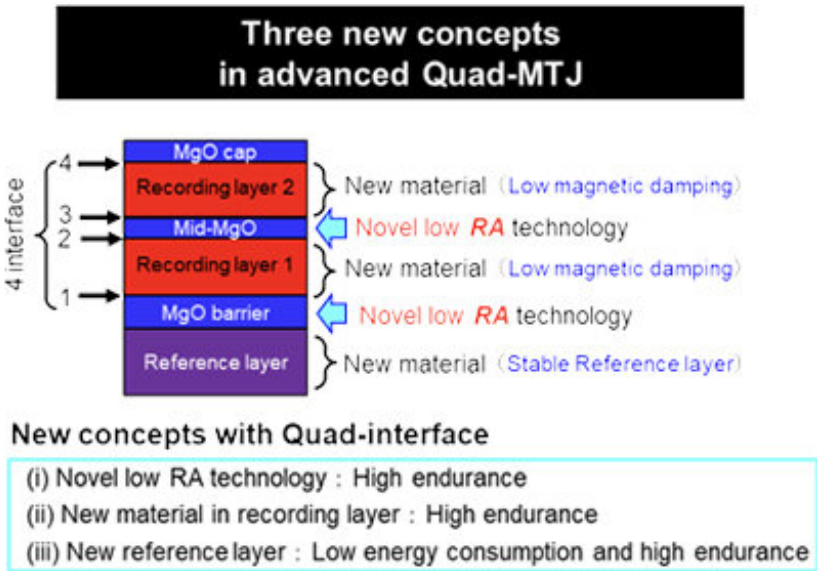


Figure 1: A schematic illustration of the new advanced Quad-MTJ technology concept. Based on Quad-interface technology with high retention over 10-years, advanced Quad-MTJ realizes a high endurance property by introducing (i) low RA MgO barrier, (ii) low magnetic dumping in recording layer, and (iii) stable reference layer. Credit: IEEE & Tohoku University

Professor Tetsuo Endoh's Group at Tohoku University's Center for Innovative Integrated Electronics has announced a new magnetic tunnel

junction (MTJ) quad-technology that provides better endurance and reliable data retention—over 10 years—beyond the 1X nm generation.

This novel Quad technology meets the design requirements for the state-of-the-art X nm complementary metal-oxide semiconductor (CMOS) node and will pave the way for ultra-low-power consumption for Internet of Things (IoT) edge-devices in mobile communication, the [automotive industry](#), consumer electronics, and industrial/infrastructure equipment.

The results will be presented in June at an international conference on semiconductor ultra-large scale integrated circuits entitled "2021 Symposia on VLSI Technology and Circuits." The conference takes place from June 13 to 19.

Developing smart societies through the use of the IoT, AI, and networks based on the next-generation mobile communication systems requires edge devices to be more power-efficient. A greater power efficiency also aids the goal of becoming carbon neutral.

Many logic circuits embedded with spin transfer-torque magnetoresistive random access memory (STT-MRAM) as a low power consumption technology. However, meeting the design rules of the X nm CMOS requires the MTJ diameter to be formed using the back end of line (BEOL) process and must fabricate at 1X nm generation.

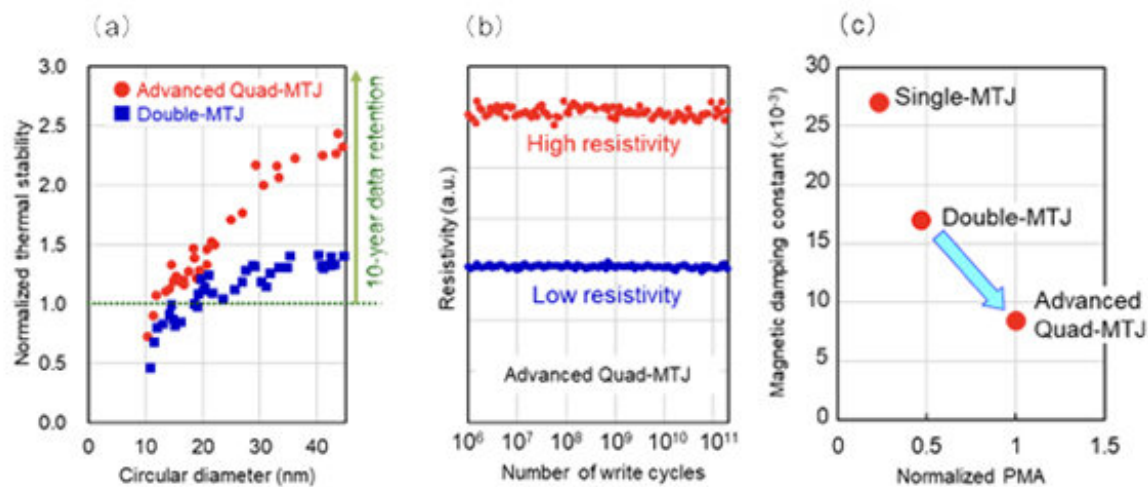


Figure 2: (a) Shows the thermal stability of the circular diameter for the novel designed advanced-Quad-interface MTJ developed in this study and the conventional Double-interface MTJ. (b) Demonstrates the number of writes cycles (endurance) of the advanced 18 nm Quad-MTJ and Double-MTJ. The endurance of advanced 18 nm Quad-MTJ exceeds at least  $6 \times 10^{11}$  due to the high write efficiency of the new Quad technology. (c) Indicates the damping constant of the novel ferromagnetic materials used for recording layers 1 and 2. The magnetic damping constant decreases in the order of Single, Double, and Quad, achieving low power consumption and high endurance. Credit: IEEE & Tohoku University

The developed Quad-interface MTJ (Quad MTJ) - the first of its kind—has three new technologies: (i) a low RA technology, (ii) a low damping material in the recording layer, and (iii) a stable reference layer.

This enabled it to have (1) better retention characteristics of over 10 years, (2) endurance that exceeded at least  $6 \times 10^{11}$ , (3) a high-speed

write operation of 10 nanoseconds, (4) a low power consumption operation of 20%, and (5) a low write error rate combined with a circular diameter of 18 nm. Additionally, the Quad-MTJ has high retention and high endurance characteristics at a 10 ns high-speed operation. This is the first time in the world that severe conditions 1—5 have been realized at the 1X nm generation.

The 18nm Quad-MTJ possesses a large capacity STT-MRAM technology that is smaller than static random access memory (SRAM). As such, it is expected to replace SRAM for the X nm generation in CMOS logic. This means that STT-MRAM's application can expand to the leading-edge logic, achieving ultra-power consumption, excellent scalability and high reliability in application processors.

**More information:** Advanced 18 nm Quad-MTJ technology overcomes dilemma of Retention and Endurance under Scaling beyond 2X nm. Conference: 2021 Symposia on VLSI Technology and Circuits

Provided by Tohoku University

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