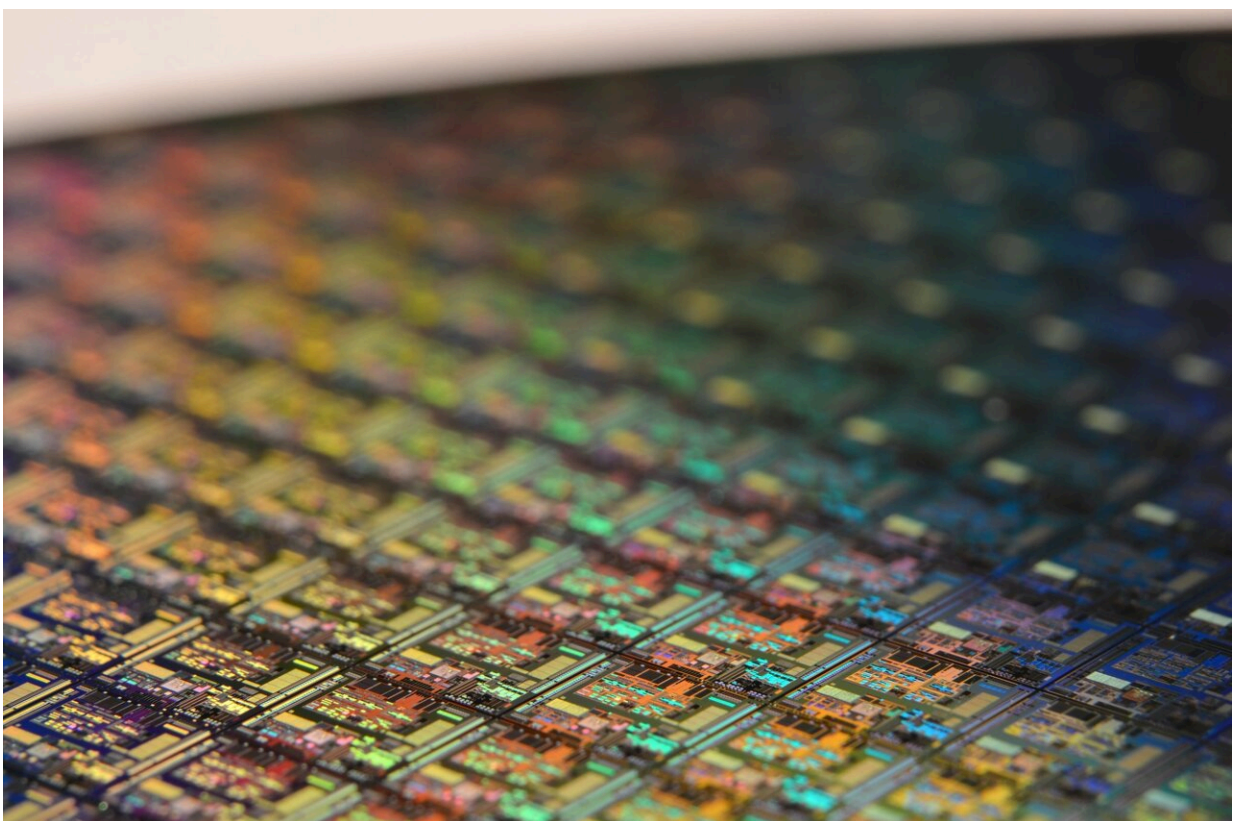


Molybdenum disulfide vertical transistors with channel lengths down to one atomic layer

June 8 2021, by Ingrid Fadelli



Credit: Unsplash

Vertical transistors, transistors with channel lengths that are dependent on a semiconductor's thickness, could be highly valuable for the

development of new generations of electronic devices. In contrast with conventional planar transistors, which are built in layers and can have all their connections on the same plane, in fact, vertical transistors might be more affordable and easier to manufacture.

So far, creating vertical devices with short channel lengths has proved to be highly challenging, primarily due to the damage to the contact region caused by high-energy metallization processes. Identifying alternative strategies to manufacture vertical transistors with shorter channel lengths is thus a crucial step in enabling the large-scale production of these devices.

Researchers at Hunan University in China have recently devised a low-energy van der Waals metal integration technique to fabricate [molybdenum disulfide](#) (MoS_2) vertical transistors with short channel lengths. Using this technique, outlined in a paper published in *Nature Electronics*, they were able to create vertical transistors with channel lengths down to one atomic layer.

"We show that molybdenum disulfide (MoS_2) vertical transistors with channel lengths down to one atomic layer can be created using a low-energy van der Waals metal integration technique," the researchers wrote in their paper. "The approach uses prefabricated metal electrodes that are mechanically laminated and transferred on top of MoS_2 /graphene vertical heterostructures, leading to vertical field-effect transistors with on-off ratios of 26 and 10^3 for channel lengths of 0.65 nm and 3.60 nm, respectively."

Liting Liu and the rest of the team at Hunan University evaluated the performance of the vertical field-effect transistors they created in a series of tests and experiments. To conduct these evaluations, they used a technique called scanning-tunneling microscopy and gathered electrical measurements at low temperatures.

"Using scanning tunneling microscopy and low-temperature [electrical measurements](#), we show that the improved electrical performance is the result of a high-quality metal-semiconductor interface, with minimized direct tunneling current and Fermi-level pinning effect," the researchers wrote in their paper.

In the initial evaluations conducted by Liu and her colleagues, the MoS₂-based vertical transistors achieved highly promising results. Compared to previously proposed vertical devices with short channel lengths, in fact, they exhibited significantly better electrical performances.

The new vertical transistors developed by this team of researchers could ultimately enable the fabrication of new types of electronic devices with shorter gate lengths. The metal integration technique proposed by the researchers could also be used by other teams to create similar vertical transistors with varying [channel](#) lengths.

In addition, the integration approach presented in the recent paper could be applied to other layered materials, such as tungsten diselenide and tungsten disulfide. This may in turn enable the fabrication of other sub-3-nm p-type and n-type vertical [transistors](#).

More information: Transferred van der Waals metal electrodes for sub-1-nm MoS₂ vertical transistors. *Nature Electronics*(2021). [DOI: 10.1038/s41928-021-00566-0](#).

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