Studying RISC-V architecture to create customized systems for space computing

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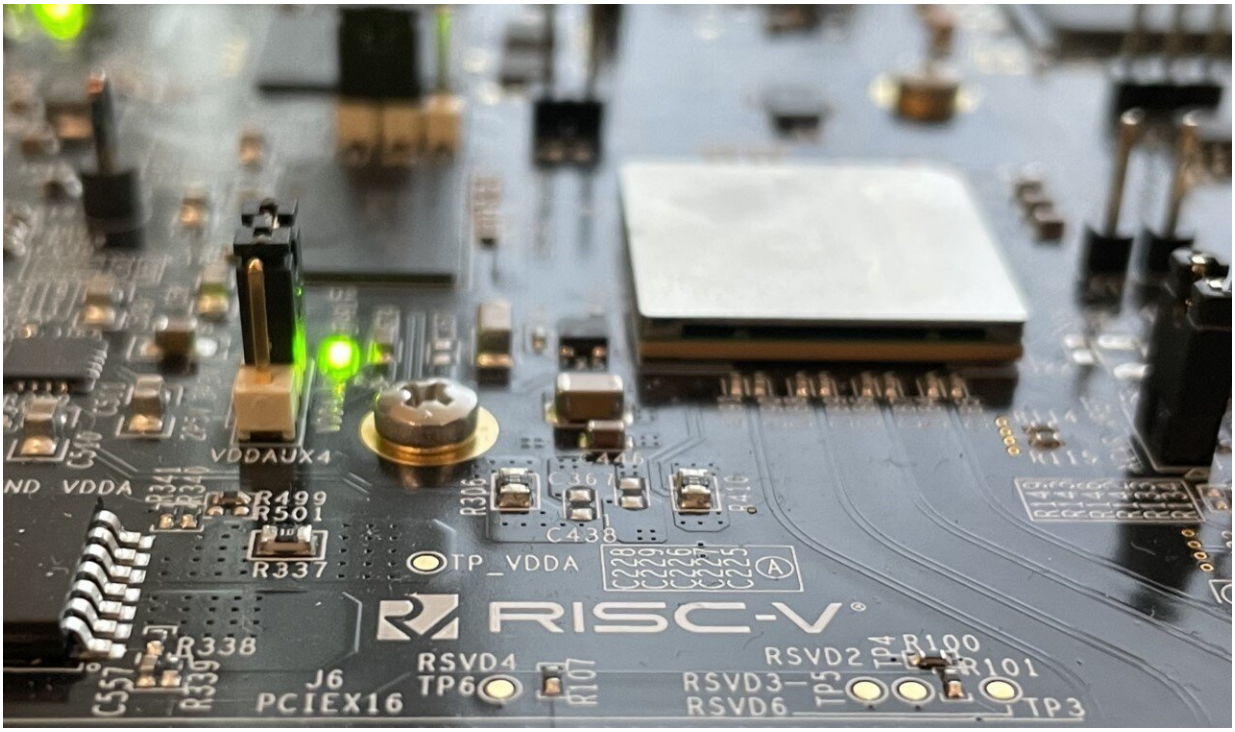

Credit: University of Pittsburgh

When choosing a processor for space computing, there are many factors that come into play: because of the rigors of a harsh environment, developers must find the optimal balance between size, weight, power and cost. An important variable in this design is the processor architecture, which can have a significant impact on balancing

performance and power consumption.

Students at the University of Pittsburgh's NSF Center for Space, High-performance, and Resilient Computing (SHREC) examined the RISC-V architecture for space computing and presented their results at the 2021 IEEE Space Computing Conference. They were awarded the Best Paper Award for Research in Space Computing for their work.

"RISC-V is exciting because it's open-source and benefits from collaborative development," said Michael Cannizzaro, lead author on the paper and an electrical and computer engineering Ph.D. student at Pitt's Swanson School of Engineering. "There is a large community, ranging from individuals to large companies, that are contributing to this development."

RISC—or Reduced Instruction Set Computer—is a more efficient approach to computing that uses a simple, optimized set of instructions compared to other architectures. RISC-V, in particular, is lauded for its modularity—a unique characteristic that sets it apart from other designs and allows users to add specialized functionality to individual systems.

"With RISC-V, the base set of instructions essentially acts as a foundation on which a processor designer can easily develop a system that includes all the features they want, without any unnecessary extras," Cannizzaro explained.

Typical architectures are proprietary and require licensing, but RISC-V's open-source structure decreases development costs and allows a wider audience of innovators to explore its applications. According to the SHREC team, RISC-V may be particularly appealing for space missions.

"The architecture's modularity means that different implementations of RISC-V can be used in a variety of space systems—from navigation and

image processing to communications and machine learning," said Evan Gretok, an electrical and computer engineering Ph.D. student at Pitt, who also contributed to the study. "However, no one can benefit from these features if the architecture itself can't perform computations in time and within the strict power consumption constraints of space—that's where our work comes in."

This research is the starting point of a more in-depth investigation into a promising new architecture that may potentially lead to a space-ready RISC-V computer.

"We are currently working on extending this work by incorporating additional architectures, processing platforms, and benchmark tests," Cannizzaro added. "These new additions will help us make the best conclusions about the RISC-V architecture and its readiness for space.

"RISC-V is moving forward at a very fast pace, and we're excited to see all the new systems that are developed with this technology in the near future."

More information: Cannizzaro, Michael James (2021) RISC-V Benchmarking for Onboard Sensor Processing. Master's Thesis, University of Pittsburgh. (Unpublished) d-scholarship.pitt.edu/40400/

Provided by University of Pittsburgh

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