

Intel applies for stacked forksheet transistor patent

January 25 2022, by Bob Yirka

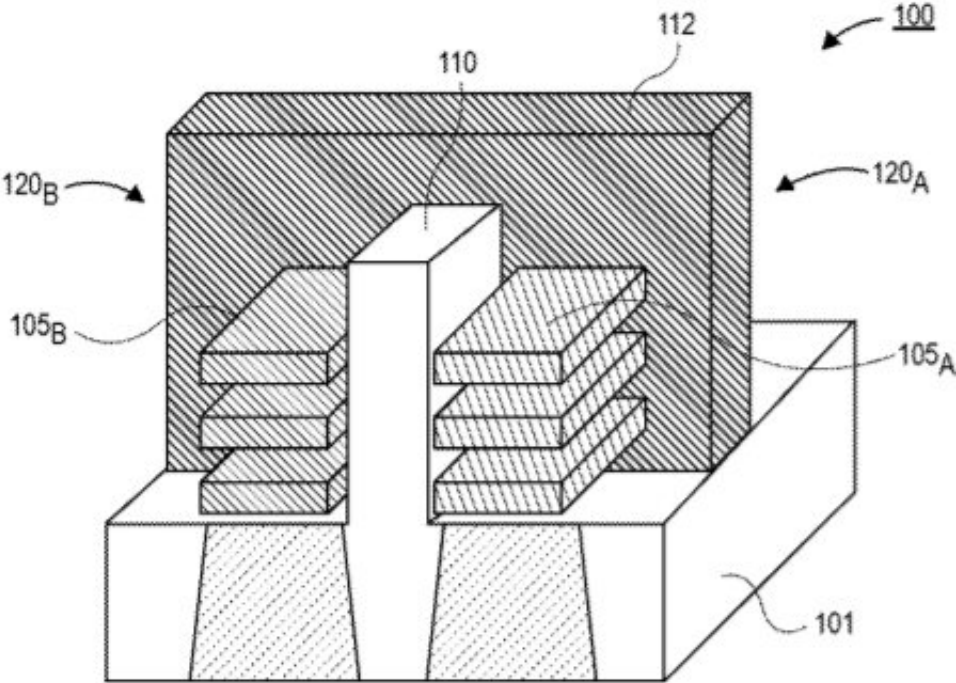


FIG. 1A

Figure 1A is a perspective view illustration of forksheet transistors, in accordance with an embodiment. Credit:

<https://www.freepatentsonline.com/20210407999.pdf>

Twitter user @Underfox3 has posted a [tweet](#) showing an application for a patent by Intel. In it, Intel has [applied for a patent](#) on a stacked forksheet transistor—a type of stacked transistor that might allow the

company to produce chips with 18 Angstrom transistors on them.

The [patent application](#) was filled out by Intel's Components Research Group and demonstrates the companies' interest in developing chips that are either faster or do more with the same amount of power. The design is described as a transistor device that is made using a vertical stack of semiconductor channels next to the edges of a backbone. Then, a second transistor, which also has a vertical stack of semiconductor channels next to a backbone is stacked on top of the first transistor.

Pursuing this stacked transistor technology allows Intel to add more [transistors](#) to a [chip](#) and achieve faster communications between transistors by giving chips the ability to send signals in three dimensions instead of two, the technology used on current chips.

Notably, Intel included a node called 20A on slides it made public recently showing the company's new node naming convention—the A stands for Angstrom. Twenty of them would be equivalent to 2 nanometers (the size refers to the distance between gates), which suggests the new transistor design (using what the company describes as RibbonFET technology) would be sub 3nm, which is the current company standard. Along with the new node naming, Intel also suggested that it would be making some refinements to the 20A, which would lead to the development of the 18A. Some in the press have suggested that the new refinement could be the application of stacked forksheeting.

Also, the word "forksheet" appears to have come from a Belgian [company](#) called Imec, which posted a document online in 2019 describing a stacked type of transistor, which they called a forksheet. Intel did not make any claims or predictions regarding the performance of their proposed forksheet transistor but Imec claimed on their posting that their design would result in a 10% speed gain or a 24% reduction in power.

More information: Patent application:
www.freepatentsonline.com/20210407999.pdf

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