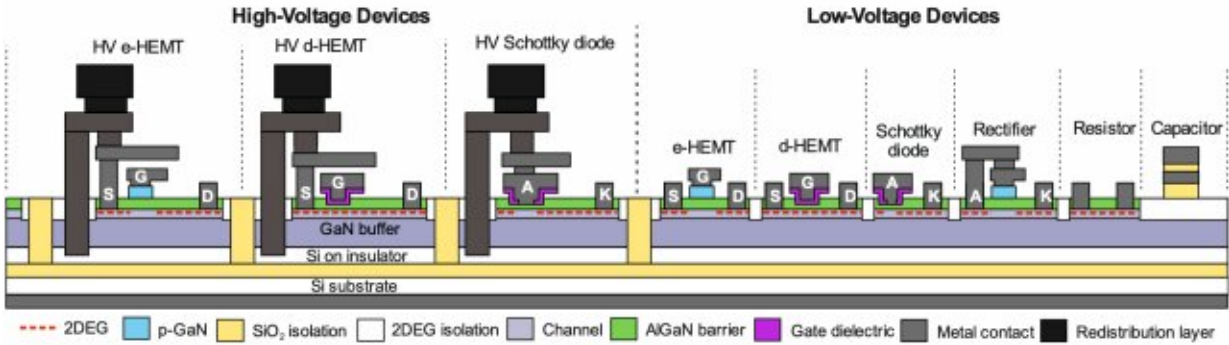


Monolithic integration of GaN components boosts power integrated circuits

March 21 2022, by Stefaan Decoutere



Schematic cross-section of IMEC 200V GaN-on-SOI Power IC technology and components. The process features monolithic co-integration of E/D mode HEMTs, Schottky diodes, resistors, capacitors, and includes advanced process modules. Credit: IMEC

For decades, silicon-based power transistors (MOSFETs, field-effect transistors) formed the backbone of power conversion systems that convert alternating current (AC) into direct current (DC) and vice versa,

or DC from low voltage to high voltage and vice versa. In the quest for alternatives that can drive up the switching speed, gallium nitride (GaN) quickly came forward as one of the leading candidate materials. The GaN/AlGaN materials system exhibits a higher electron mobility and higher critical electric field for breakdown. Combined with the high electron mobility transistor (HEMT) architecture, it results in devices and ICs that feature higher breakdown strength, faster switching speed, lower conductance losses and a smaller footprint than comparable silicon solutions.

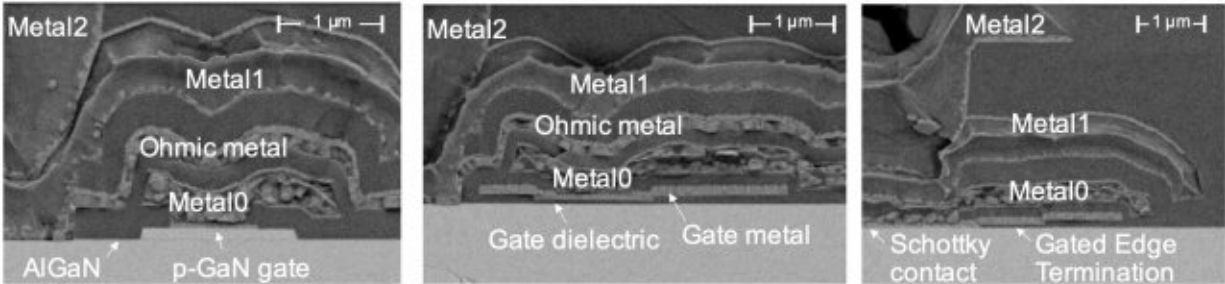
Today, most GaN power systems are formed from multiple chips. GaN-based devices are assembled as discrete components before they are united on a printed circuit board. The downside of that approach is the presence of parasitic inductances that affects the performance of the devices. "Take a driver, for example. Discrete transistors with drivers on a separate chip suffer a lot from parasitic inductances between the output stages of the driver and the input of the transistor, and in the switching node of half bridges. GaN HEMTs have very high switching speed which leads to ringing, an unwanted oscillation of the signal, when the parasitic inductance is not suppressed. The best way to reduce the parasitics and exploit the superior switching speed of GaN is to integrate both driver and HEMT on the same chip," explains Stefaan Decoutere.

"At the same time, it reduces the dead-time control between two transistors in a half bridge, where one transistor has to switch off just as the other one switches on. During the time in between, there is a short-circuit between the [power source](#) and the ground, or dead time. Integrating all components on chip will address the ringing, reduce dead time, and ultimately improve the power efficiency of your converter."

Co-integration of d-mode HEMTs

Imec has already made tremendous progress monolithically integrating

building blocks on a silicon-on-insulator (SOI) substrate such as drivers, half bridges, and control/protection circuits. Now, researchers have succeeded in adding two sought-after components to the portfolio: d-mode (depletion-mode) HEMTs and Schottky diodes.



Process cross-sections of the high-voltage components fabricated on 200 mm GaN-on-SOI substrates (a) e-mode pGaN-HEMT (b) d-mode MIS-HEMT, (c) Schottky barrier diode. All devices include metal field plates based on front-end and interconnect metal layers and separated by dielectric layers. Credit: IMEC

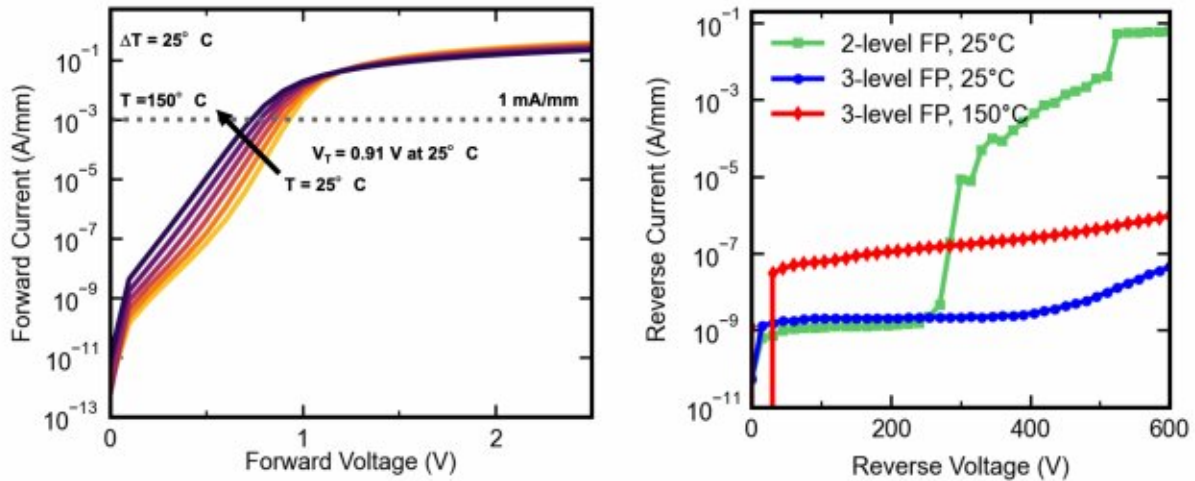
One of the main hurdles to boost the full performance of GaN power ICs remains finding a suitable solution for the lack of p-channel devices in GaN with acceptable performance. CMOS technology uses complementary and more symmetrical pairs of p- and n-type FETs, based on the mobilities of holes and electrons for both types of FETs.

However, in GaN, the mobility of holes is about 60 times worse than that of electrons; in silicon this is only a factor of 2. That means a p-channel device, where holes are the principal carriers, would be 60 times larger than the n-channel counterpart and highly inefficient. A widespread alternative is replacing the P-MOS with a resistor. Resistor-Transistor Logic (RTL) has been employed for GaN ICs but shows trade-offs between switching time and power consumption.

"We have improved the performance of GaN ICs by co-integrating d-mode HEMTS on our functional e-mode HEMT platform on SOI. Enhancement and depletion mode refer to an ON (d-mode) or OFF (e-mode) state at zero source voltage, resulting in a current flow (or not) in the transistor. We expect that taking the step from RTL to direct-coupled FET logic will improve speed and reduce the power dissipation of the circuits," says Stefaan Decoutere.

Schottky diodes with low leak currents

The integration of a Schottky barrier diode further boosted the power efficiency of the GaN power ICs. In comparison with Si diodes, they can withstand higher voltages for the same ON-state resistance or lower ON-state resistance for the same breakdown voltage. "The challenge in making Schottky barrier diodes is to obtain low turn-on voltage and at the same time a low leakage level. Unfortunately, when you aim for lower turn-on voltages, you will end up with a small barrier to hold off the leakage current. And Schottky diodes are notorious for having high leak currents. Imec's proprietary Gate-Edge-Terminated Schottky Barrier Diode architecture (GET-SBD) results in a low turn-on voltage of about 0.8 Volt, while at the same time reduces the leakage current several orders of magnitude in comparison with conventional GaN Schottky barrier diodes," adds Stefaan Decoutere.



Characteristics of manufactured GET-SBDs showing (left) low turn-on voltage of 0.91V at 25°C in semi-log scale, and (right) low reverse leak currents (2 nA/mm for 25°C) for two different anode field plates configurations evaluated at 25 and 150°C . Credit: IMEC

Fast switches and high voltages

GaN is the go-to material for high power applications because the critical voltage that induces breakdown of the transistor (breakdown voltage) lies 10 times higher than in silicon. But also for low-power applications GaN still has an edge over silicon because of its superior switching speed. "The GaN-based ICs we create, open the way towards smaller and more efficient DC/DC converters and Point-of-Load (PoL) converters. A smartphone, tablet or laptop for example, contain chips that work on different voltages, so they require AC/DC converters for charging the battery and PoL converters inside the devices for generating

the different voltages. These components not only consist of a switch but also transformers, capacitors, and inductors. The faster the transistor can switch, the smaller these components become, ultimately resulting in a more compact and low-cost system for the same power."

Stefaan Decoutere: "Fast battery chargers form the largest market for GaN today, followed by power supplies for servers, automotive industry and renewable energy. It is expected that the power supplies using GaN are at the system level more reliable. They are smaller in form factor and weight, reducing the bill of materials and hence the cost."

Vertical devices under research

"We will focus on improving the performance of the existing platform and perform further reliability tests. We currently offer a 200V and 650V platform for prototyping, soon to be followed by 100V. For GaN-ICs with integrated components, a 1200V high-power platform may not yield significant improvements. The higher the voltage, the slower the components become. Therefore, it may not be necessary to integrate the driver on chip; simulations will tell us."

"At the same time, we are looking into alternatives for discrete 1200V devices, enabling GaN technology for highest voltage [power](#) applications such as electric cars. Transistors with a lateral topology are the dominant GaN device architecture today. These devices have their three terminals (source, gate, and drain) at the surface in the same plane, so the electrical field is lateral, spanning the GaN buffer layers and partly the backend (metallization, oxide). In a vertical device, the source and gate are at the surface, while the drain is at the bottom of the epi stack. The electrical field in that case flows through the whole stack. It is the source-drain separation that determines the breakdown [voltage](#) of the device, and a larger separation safeguards the channel from breakdown. However, larger distances between a laterally-placed source and drain

result in larger devices. Because the chips for 1200V devices would become too large, lateral architectures are usually advised up to 650V maximum. For a vertical [device](#), on the contrary, going to higher voltages boils down to creating a thicker epi stack because source and drain are located on different ends of the stack. The chip's surface area doesn't increase," concludes Stefaan Decoutere.

More information: These results of Cosnier T et al. 200V GaN-on-SOI smart power platform for monolithic GaN power ICs were presented at the IEDM 2021 conference. The conference paper can be requested via [the form](#)

Provided by IMEC

Citation: Monolithic integration of GaN components boosts power integrated circuits (2022, March 21) retrieved 26 April 2024 from <https://techxplore.com/news/2022-03-monolithic-gan-components-boosts-power.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.