# Creating sub-1-nm gate lengths for MoS2 transistors

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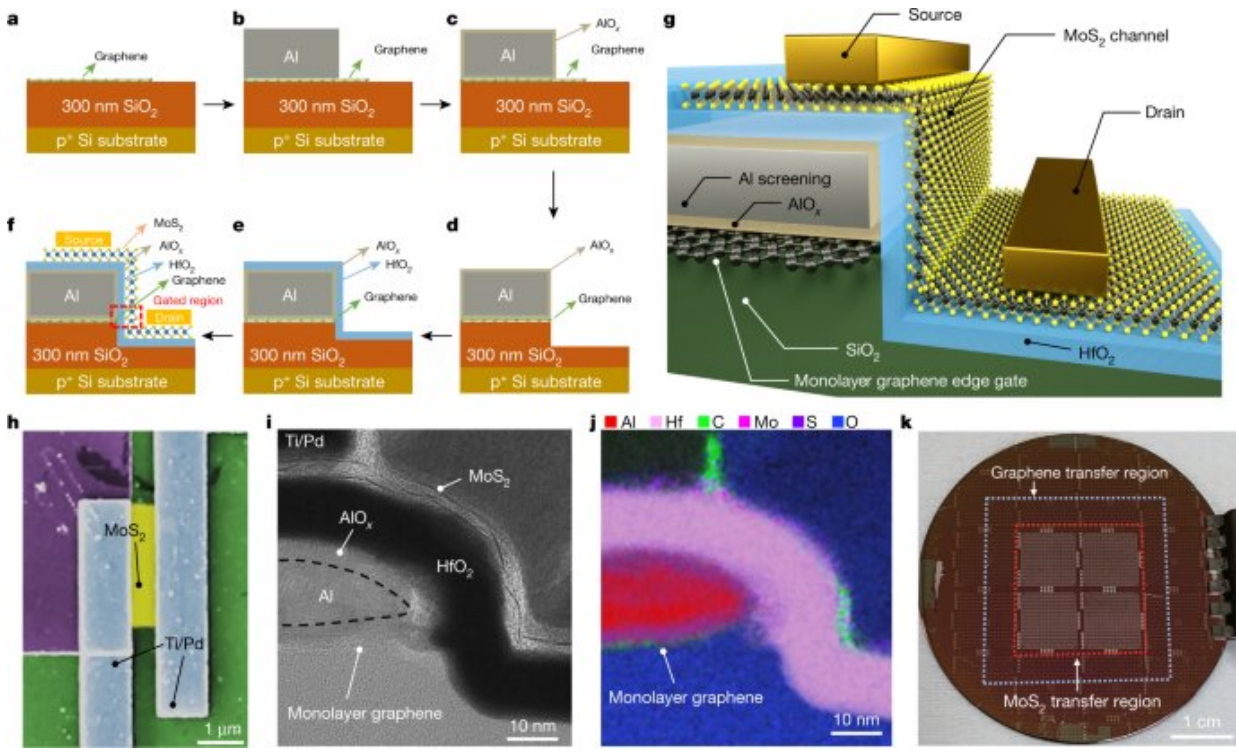


The 0.34 nm gate-length side-wall monolayer MoS2 transistor device structure and characterization. Credit: *Nature* (2022). DOI: 10.1038/s41586-021-04323-3

A team of researchers working at Tsinghua University in China has created a sub-1-nm gate in a $MoS_2$ transistor. In their paper published in the journal *Nature*, the group outlines how they created the super tiny gate and explains why they believe it will be difficult for anyone to beat

their record.

For most of the history of microcomputing, Moore's Law has held up—researchers and engineers have managed to double the speed and capability of computers regularly by reducing the size of their components. But more recently, it has grown increasingly difficult to make components smaller as scientists now run into physical limitations. In this new effort, the researchers believe they may have bumped up against the ultimate limit—they have built a gate that is just one atom in length.

At their most basic, transistors are a source and a drain, with a gate controlling the flow of electricity between them. It switches on and off depending on how much electricity is applied. The push to reduce the size of the components has led to the testing of materials such as carbon nanotubes, which are approximately 1nm, for use as gates. In this new effort, the researchers have unrolled the carbon nanotube and used its graphene edge as the gate—reducing its length to just 0.34 nm.

To make their gate, and a source and drain to go along with it, the researchers created a multiple-layer sandwich of materials. The bottom silicon layer serves as a base, which was covered by a layer of graphene, followed by a layer of aluminum oxide. Next, they etched the material to remove the top layers from half of their transistor, leaving a stairstep configuration to expose the edge of the graphene layer, allowing its use as a gate. They then covered both parts of the transistor with a layer of hafnium oxide to create a channel between the source and drain and through the gate. Then finally, they added two metal electrodes, one on the upper part of the step to serve as the source and one on the lower part of the step to serve as the drain.

**More information:** Fan Wu et al, Vertical MoS2 transistors with sub-1-nm gate lengths, *Nature* (2022). DOI:

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