Researchers develop a scaled-up spintronic probabilistic computer

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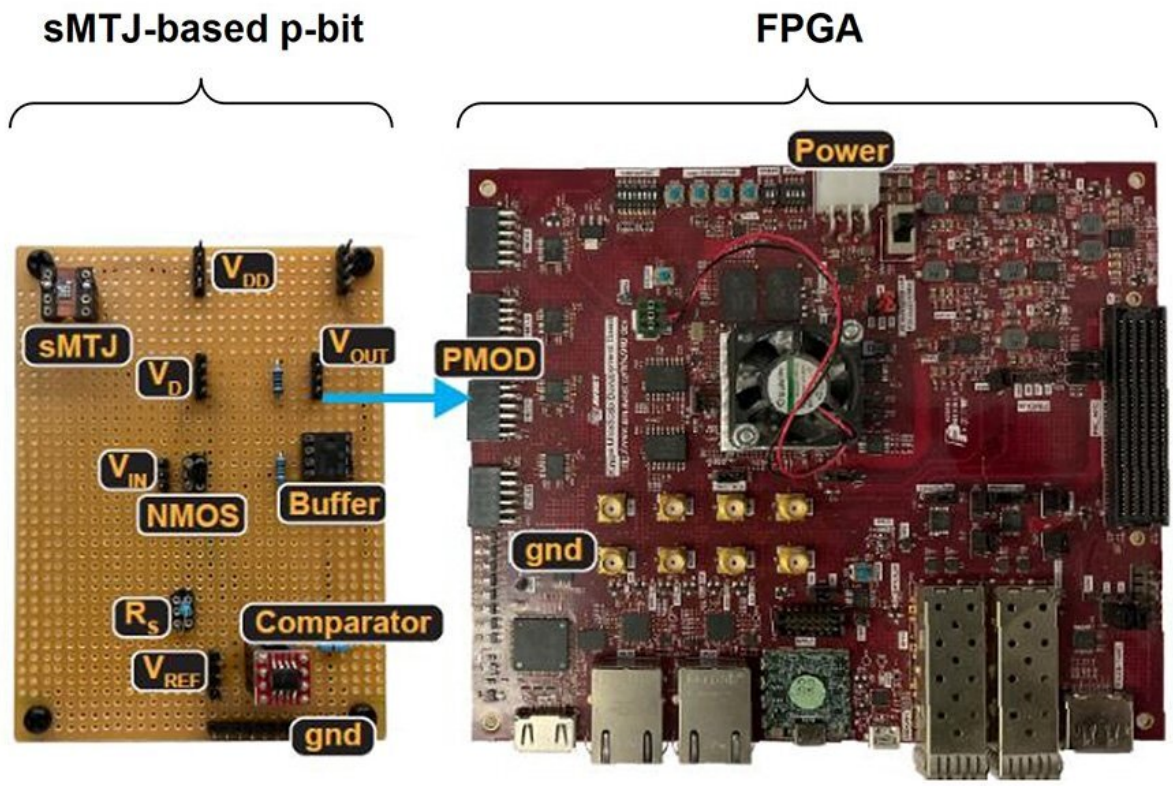


A photograph of the constructed heterogeneous p-computer consisting of stochastic magnetic tunnel junction (sMTJ) based probabilistic bit (p-bit) and field-programmable gate array (FPGA). Credit: Kerem Camsari, Giovanni Finocchio, and Shunsuke Fukami et al.

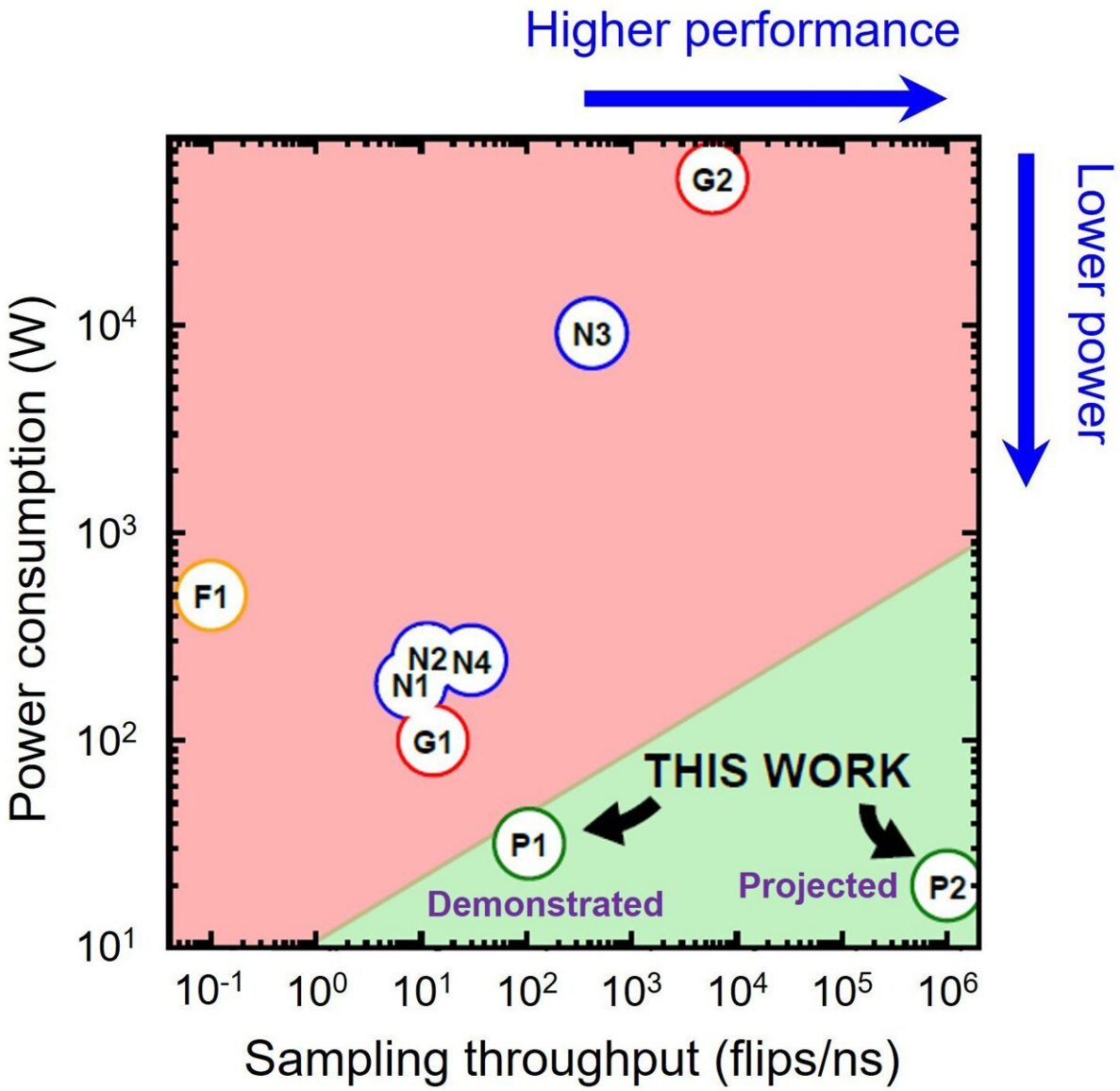
Researchers at Tohoku University, the University of Messina, and the

University of California, Santa Barbara (UCSB) have developed a scaled-up version of a probabilistic computer (p-computer) with stochastic spintronic devices that is suitable for hard computational problems like combinatorial optimization and machine learning.

Moore's law predicts that computers get faster every two years because of the evolution of semiconductor chips. While this is what has historically happened, the continued evolution is starting to lag. The revolutions in machine learning and artificial intelligence means much higher computational ability is required. Quantum computing is one way of meeting these challenges, but significant hurdles to the practical realization of scalable quantum computers remain.

A p-computer harnesses naturally stochastic building blocks called probabilistic bits (p-bits). Unlike bits in traditional computers, p-bits oscillate between states. A p-computer can operate at room-temperature and acts as a domain-specific computer for a wide variety of applications in machine learning and artificial intelligence. Just like quantum computers try to solve inherently quantum problems in quantum chemistry, p-computers attempt to tackle probabilistic algorithms, widely used for complicated computational problems in combinatorial optimization and sampling.

Recently, researchers from Tohoku University, Purdue University, and UCSB have shown that the p-bits can be efficiently realized using suitably modified spintronic devices called stochastic magnetic tunnel junctions (sMTJ). Until now, sMTJ-based p-bits have been implemented at small scale; and only spintronic p-computer proof-of-concepts for combinatorial optimization and machine learning have been demonstrated.



A comparison of probabilistic accelerators as a function of sampling throughput and power consumption. Graphics Processing Units (GPUs) [plotted as N1-N4], Tensor Processing Units (TPUs) [plotted as G1-G2], and simulated annealing machine [plotted as F1] are compared with probabilistic computers, where demonstrated value and projected value are plotted as P1 and P2, respectively. Credit: Kerem Camsari, Giovanni Finocchio, and Shunsuke Fukami et al.

The research group has presented two important advances at the 68th International Electron Devices Meeting (IEDM) on December 6th, 2022.

First, they have shown how sMTJ-based p-bits can be combined with conventional and programmable semiconductor chips, namely, Field-Programmable-Gate-Arrays (FPGAs). The "sMTJ + FPGA" combination allows much larger networks of p-bits to be implemented in hardware, going beyond the earlier small-scale demonstrations.

Second, the probabilistic emulation of a quantum algorithm, simulated quantum annealing (SQA), has been performed in the heterogeneous "sMTJ + FPGA" p-computers with systematic evaluations for hard combinatorial optimization problems.

The researchers also benchmarked the performance of sMTJ-based p-computers with that of classical computing hardware, such as graphics processing units (GPUs) and Tensor Processing Units (TPUs). They showed that p-computers, utilizing a high-performance sMTJ previously demonstrated by a team from Tohoku University, can achieve massive improvements in throughput and power consumption than conventional technologies.

"Currently, the 's-MTJ + FPGA' p-computer is a prototype with discrete components," said Professor Shunsuke Fukami, who was part of the research group. "In the future, integrated p-computers that make use of semiconductor process-compatible magnetoresistive random access memory (MRAM) technologies may be possible, but this will require a co-design approach, with experts in materials, physics, circuit design and algorithms needing to be brought in."

More information: Experimental evaluation of simulated quantum annealing with MTJ-augmented p-bits. 68th Annual IEEE International Electron Devices Meeting

Provided by Tohoku University