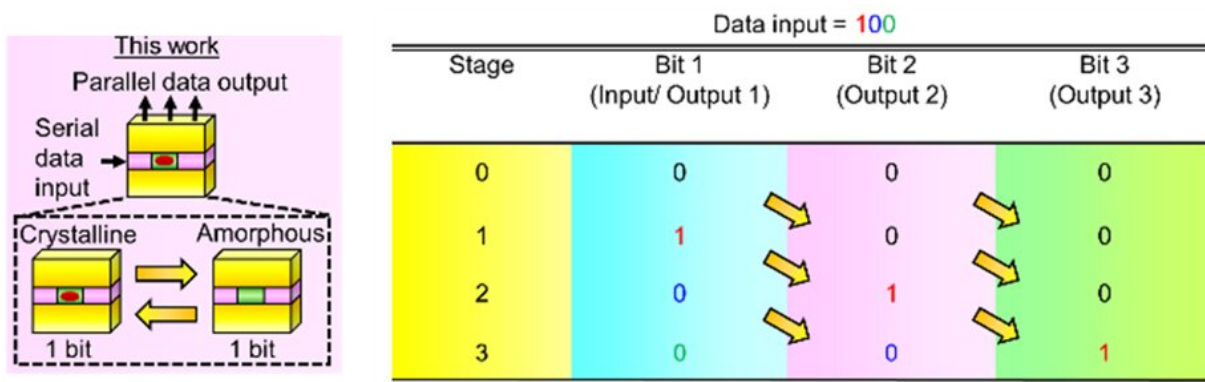


# Researchers develop a novel reconfigurable device that can bridge the gap between processor and memory

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Schematic representation of the data loading to and retrieval from the device that occurs in the serial model and parallel mode, respectively (left panel) and the table showing changes of the states in the three bits during operations (right panel). Credit: SUTD

Developing energy efficient high performing computing devices (i.e., devices that not only consume little power, but also compute information rapidly) is a key goal of edge computing research. Combining the memory components and units that perform shift register operations is a potential way to achieve this goal.

Most computing devices are made up of a physically separate [memory](#)

component and processing unit. To substantially simplify these devices and reduce its power consumption, a device that can potentially perform both functions efficiently—the shift register-in-memory architecture—has been developed.

Conventional shift register-in-memory architectures have limitations, although some of these architectures show promising results. The limitations include the use of many devices and the requirement to convert the [electrical resistance](#) to electric signals.

Based on phase-change alloys, [materials](#) that switch reversibly between the glassy [amorphous state](#) and the ordered crystal state, researchers at the Singapore University of Technology and Design (SUTD) have developed a new reconfigurable shift register-in-memory architecture. Their device works both as a reconfigurable memory component and as a programmable shift register and has been introduced in a paper published in *Advanced Intelligent Systems*.

The term "material (M) state-based shift register" was used to describe the shift register-in-memory device developed by the researchers. The four material states (i.e., the amorphous state, fully [crystalline state](#), partially crystallized state and primed state) of the phase-change material (representing different shift register/ memory modes) were used to operate the device.

The device can be switched to perform either shift register or memory functions and is easily programmable due to its special design. The researchers showed that the device performed impressively for both functions in preliminary tests.

"When operating as a memory, the device can be switched from the disordered glass state to crystalline state with 1.9 ns pulses, which is about one-third shorter than those of existing devices with germanium

antimony telluride layers doped with nitrogen; and exhibit a resetting energy of 2 pJ. When operating as a shift register, the [device](#) can be switched between the serial-in–serial-out mode to serial-in–parallel-out mode, with a [single cell](#), and exhibit many resistance levels, which has not been shown before," said SUTD's Assistant Professor Desmond Loke, who is the principal investigator of the study.

To substantially reduce the [power consumption](#), the new shift register-in-memory architecture proposed by the research team could be used to design a wide range of high-performance electronic systems in the future. The M state-based shift registers could be applied to a variety of operation schemes and computations, although for the purpose of this research, the researchers have shown that these devices are able to perform shift register operations successfully.

**More information:** Shao-Xiang Go et al, Toward Single-Cell Multiple-Strategy Processing Shift Register Powered by Phase-Change Memory Materials, *Advanced Intelligent Systems* (2023). [DOI: 10.1002/aisy.202200353](#)

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