Novel architecture can reduce noise-induced jitters in digital technology

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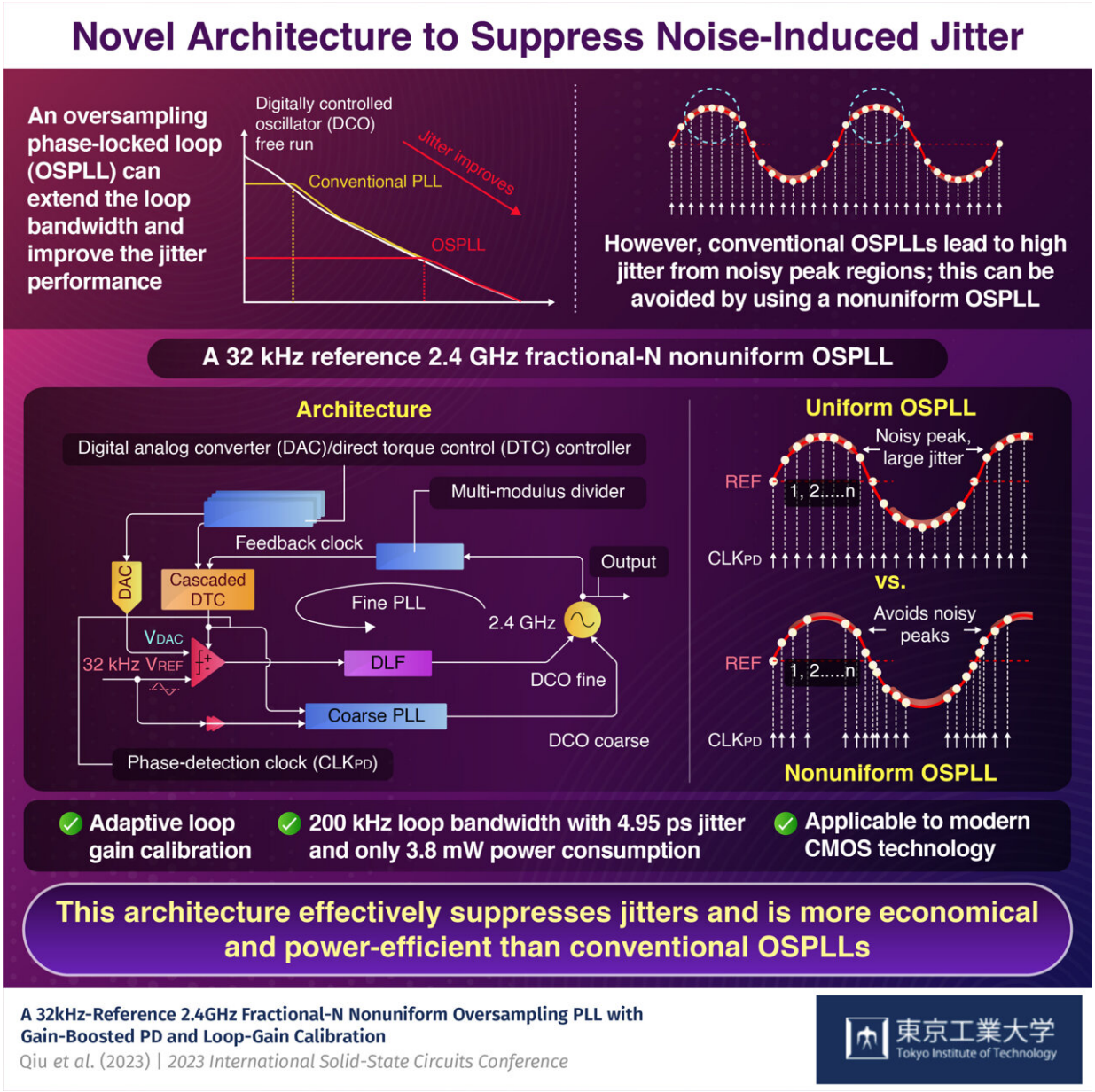

Credit: Tokyo Tech

The efficacy and efficiency of modern electronic devices often depend on their signal noise and jitter. Jitter is the fluctuation or deviation of the signal waveform in a high-frequency digital signal. There are many conventional methods to mitigate jitter and boost the performance characteristics of a device. One common method is to use an oversampling phase-locked loop (OSPPL). An OSPLL can extend the loop bandwidth and result in improved jitter performance.

Now, while they present many benefits, the use of conventional OSPLLs leads to high jitter from noisy peak regions, as the peak regions have a smaller gradient. The slow reference slope of a conventional 32 kHz signal introduces a large jitter and results in a larger attributed time error.

This disadvantage has thus far hindered the broader use of OSPLLs. Now a team of scientists from Tokyo Institute of Technology (Tokyo Tech) have demonstrated how this can be avoided by using a non-uniform OSPLL.

Professor Kenichi Okada, who led the research team, further explains the development: "Our novel over-sampling architecture provides a low-jitter, 2.4 GHz fractional-N PLL using a 32 kHz reference. The loop bandwidth of conventional PLLs is theoretically limited to 1/10th of the reference frequency, by Gardner's stability theory. This narrow loop bandwidth causes jitter degradation. Our non-uniform over-sampling PLL can increase the loop bandwidth by 60 times and can efficiently suppress jitters."

The newly ideated device architecture allows for an adaptive loop gain

calibration. By automatically performing the loop gain calibration for each sampling point, the jitter can be minimized.

"Our device's performance is highlighted by its 200 kHz loop bandwidth with 4.95 ps jitter. At these parameters, the device only consumes 3.8 mW of power. Moreover, it can be integrated with CMOS technologies, making it a particularly attractive prospect for the ever-growing electronics industry," adds Junjun Qiu from Tokyo Tech, the lead author of their study.

This paradigm-shifting architecture is also more economical and power efficient than conventional OSPLLs, owing to reduced jitter and a higher and cleaner signal.

The paper is published as part of the *2023 International Solid-State Circuits Conference*.

More information: Junjun Qiu et al, A 32kHz-Reference 2.4GHz Fractional-N Nonuniform Oversampling PLL with Gain-Boosted PD and Loop-Gain Calibration, *2023 International Solid-State Circuits Conference (ISSCC)* (2023).

Provided by Tokyo Institute of Technology