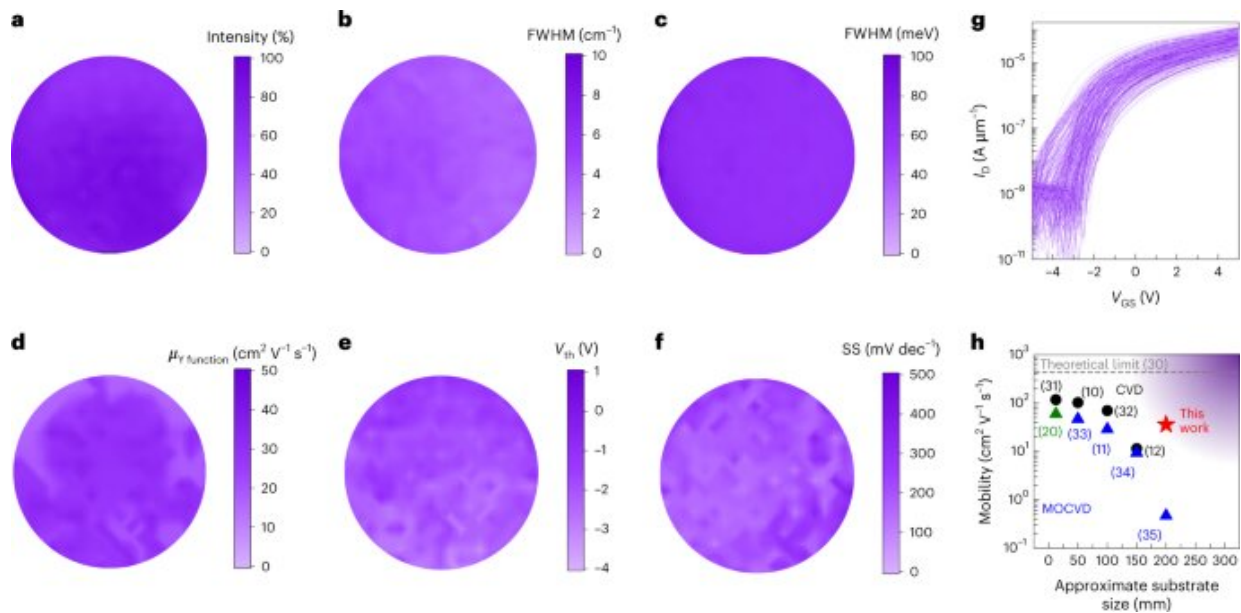


Engineers 'grow' atomically thin transistors on top of computer chips

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Uniformity characterization of the 200 mm monolayer MoS₂ synthesized at low temperature. Credit: *Nature Nanotechnology* (2023). DOI: 10.1038/s41565-023-01375-6

Emerging AI applications, like chatbots that generate natural human language, demand denser, more powerful computer chips. But semiconductor chips are traditionally made with bulk materials, which are boxy 3D structures, so stacking multiple layers of transistors to create denser integrations is very difficult.

However, semiconductor transistors made from ultrathin 2D materials, each only about three atoms in thickness, could be stacked up to create more powerful chips. To this end, MIT researchers have now demonstrated a [novel technology](#) that can effectively and efficiently "grow" layers of 2D transition metal dichalcogenide (TMD) materials directly on top of a fully fabricated silicon chip to enable denser integrations.

Growing 2D materials directly onto a silicon CMOS wafer has posed a major challenge because the process usually requires temperatures of about 600 degrees Celsius, while silicon transistors and circuits could break down when heated above 400 degrees. Now, the interdisciplinary team of MIT researchers has developed a low-temperature growth process that does not damage the chip. The technology allows 2D semiconductor transistors to be directly integrated on top of standard silicon circuits.

In the past, researchers have grown 2D materials elsewhere and then transferred them onto a chip or a wafer. This often causes imperfections that hamper the performance of the final devices and circuits. Also, transferring the material smoothly becomes extremely difficult at wafer-scale. By contrast, this new process grows a smooth, highly uniform layer across an entire 8-inch wafer.

The new technology is also able to significantly reduce the time it takes to grow these materials. While previous approaches required more than a day to grow a single layer of 2D materials, the new approach can grow a uniform layer of TMD material in less than an hour over entire 8-inch wafers.

Due to its rapid speed and high uniformity, the new technology enabled the researchers to successfully integrate a 2D material layer onto much larger surfaces than has been previously demonstrated. This makes their

method better-suited for use in commercial applications, where wafers that are 8 inches or larger are key.

"Using 2D materials is a powerful way to increase the density of an integrated circuit. What we are doing is like constructing a multistory building. If you have only one floor, which is the conventional case, it won't hold many people. But with more floors, the building will hold more people that can enable amazing new things. Thanks to the heterogenous integration we are working on, we have silicon as the first floor and then we can have many floors of 2D materials directly integrated on top," says Jiadi Zhu, an [electrical engineering](#) and computer science graduate student and co-lead author of a paper on this new technique.

Zhu wrote the paper with co-lead-author Ji-Hoon Park, an MIT postdoc; corresponding authors Jing Kong, professor of electrical engineering and computer science (EECS) and a member of the Research Laboratory for Electronics; and Tomás Palacios, professor of EECS and director of the Microsystems Technology Laboratories (MTL); as well as others at MIT, MIT Lincoln Laboratory, Oak Ridge National Laboratory, and Ericsson Research. The paper appears today in *Nature Nanotechnology*.

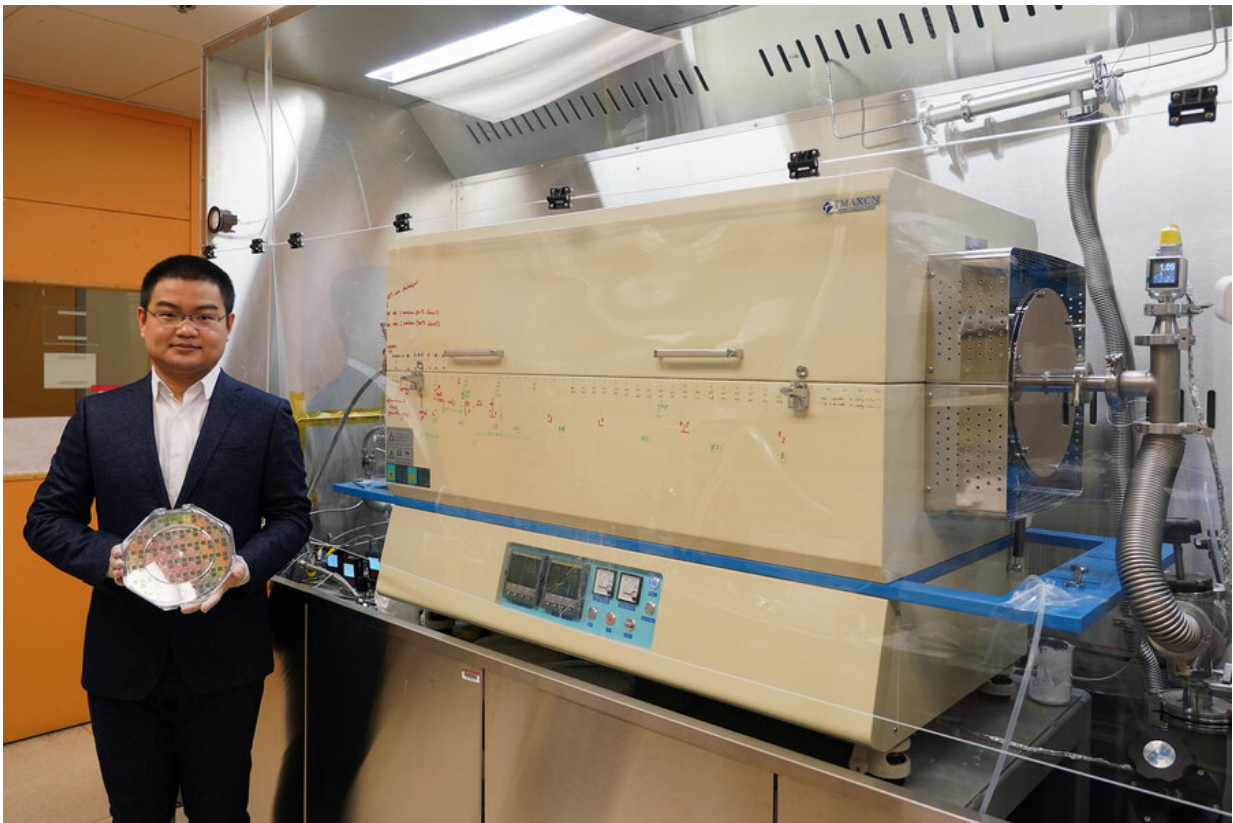
Slim materials with vast potential

The 2D material the researchers focused on, [molybdenum disulfide](#), is flexible, transparent, and exhibits powerful electronic and photonic properties that make it ideal for a semiconductor transistor. It is composed of a one-atom layer of [molybdenum](#) sandwiched between two atoms of sulfide.

Growing thin films of molybdenum disulfide on a surface with good uniformity is often accomplished through a process known as metal-organic chemical vapor deposition (MOCVD). Molybdenum

hexacarbonyl and diethylene sulfur, two organic chemical compounds that contain molybdenum and [sulfur atoms](#), vaporize and are heated inside the reaction chamber, where they "decompose" into smaller molecules. Then they link up through [chemical reactions](#) to form chains of molybdenum disulfide on a surface.

But decomposing these molybdenum and sulfur compounds, which are known as precursors, requires temperatures above 550 degrees Celsius, while silicon circuits start to degrade when temperatures surpass 400 degrees.



Graduate student Jiadi Zhu holding an 8-inch CMOS wafer with molybdenum disulfide thin film. On the right is the furnace the researchers developed, which enabled them to "grow" a layer of molybdenum disulfide onto the wafer using a low-temperature process that did not damage the wafer. Credit: Jiadi Zhu et al

So, the researchers started by thinking outside the box—they designed and built an entirely new furnace for the metal-organic chemical vapor deposition process.

The oven consists of two chambers, a low-temperature region in the front, where the silicon wafer is placed, and a high-temperature region in the back. Vaporized molybdenum and sulfur precursors are pumped into the furnace. The molybdenum stays in the low-temperature region, where the temperature is kept below 400 degrees Celsius—hot enough to decompose the molybdenum precursor but not so hot that it damages the silicon chip.

The sulfur precursor flows through into the high-temperature region, where it decomposes. Then it flows back into the low-temperature region, where the chemical reaction to grow molybdenum disulfide on the surface of the wafer occurs.

"You can think about decomposition like making black pepper—you have a whole peppercorn and you grind it into a powder form. So, we smash and grind the pepper in the high-temperature region, then the powder flows back into the low-temperature region," Zhu explains.

Faster growth and better uniformity

One problem with this process is that silicon circuits typically have aluminum or copper as a top layer so the chip can be connected to a package or carrier before it is mounted onto a printed circuit board. But sulfur causes these metals to sulfurize, the same way some metals rust when exposed to oxygen, which destroys their conductivity. The researchers prevented sulfurization by first depositing a very thin layer of passivation material on top of the chip. Then later they could open the passivation layer to make connections.

They also placed the silicon wafer into the low-temperature region of the furnace vertically, rather than horizontally. By placing it vertically, neither end is too close to the high-temperature region, so no part of the wafer is damaged by the heat. Plus, the molybdenum and sulfur gas molecules swirl around as they bump into the vertical chip, rather than flowing over a horizontal surface. This circulation effect improves the growth of molybdenum disulfide and leads to better material uniformity.

In addition to yielding a more uniform layer, their method was also much faster than other MOCVD processes. They could grow a layer in less than an hour, while typically the MOCVD growth process takes at least an entire day.

Using the state-of-the-art MIT.Nano facilities, they were able to demonstrate high material uniformity and quality across an 8-inch silicon wafer, which is especially important for industrial applications where bigger wafers are needed.

"By shortening the growth time, the process is much more efficient and could be more easily integrated into industrial fabrications. Plus, this is a silicon-compatible low-temperature process, which can be useful to push 2D materials further into the semiconductor industry," Zhu says.

In the future, the researchers want to fine-tune their technique and use it to grow many stacked layers of 2D transistors. In addition, they want to explore the use of the low-temperature growth process for flexible surfaces, like polymers, textiles, or even papers. This could enable the integration of semiconductors onto everyday objects like clothing or notebooks.

"This work made an important progress in the synthesis technology of monolayer molybdenum disulfide material," says Han Wang, the Robert

G. and Mary G. Lane Endowed Early Career Chair and Associate Professor of Electrical and Computer Engineering and Chemical Engineering and Materials Science at the University of Southern California, who was not involved with this research. "The new capability of low thermal budget growth on an 8-inch scale enables the back-end-of-line integration of this material with silicon CMOS technology and paves the way for its future electronics application."

More information: Jiadi Zhu et al, Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform, *Nature Nanotechnology* (2023). [DOI: 10.1038/s41565-023-01375-6](https://doi.org/10.1038/s41565-023-01375-6)

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