An ultra-high-density and energy-efficient content addressable memory design based on 3D-NAND flash

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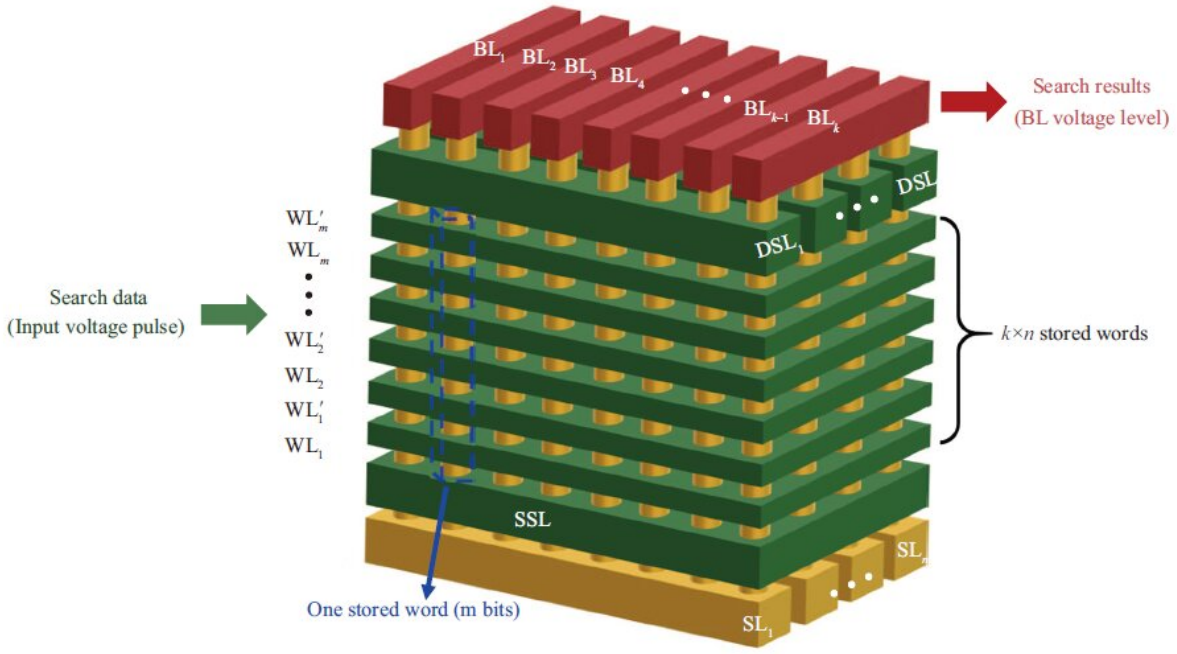

Structure of the proposed CAM design based on a 3D-NAND flash array with k×n stored words of m bits. Credit: Science China Press

Data-intensive computing applications such as pattern recognition, video processing, database engines and network routers have drastically increased due to the rapid development of big data and artificial intelligence (AI), which pose stringent requirements for storing and

processing massive data resources.

Because of the different working schemes from random access memory (RAM) and powerful functionality of high parallelism and fast speed, content addressable memory (CAM) provides an excellent solution to data-intensive computing systems. However, the existing conventional CMOS-based CAM designs prevent further development in data-intensive computing systems because of an excessively large circuit area and nontrivial standby power consumption as the scaling down of technology.

A novel 3D-NAND-based CAM design with ultra-high density and low power is proposed for data-intensive computing by Haozhang Yang and co-authors from Peking University. The specific significance and novelty are summarized as follows:

1) The proposed CAM design employs two adjacent NAND transistors in the word line direction to constitute one CAM cell. The data stored in the CAM cell are determined by the threshold voltage of two transistors together. When employing a 16-layer 3D-NAND array, the energy consumption (0.196 fJ/bit/search) is lower than the conventional SRAM based TCAMs (0.58 fJ/bit/search in 32 nm technology), and the cell density is 157 times higher than that because of 3D stacking feature.

2) A multi-level CAM design based on 3D-NAND flash is proposed to boost the cell density and expands the functionality, which stores several logic states in one CAM cell. Simulation results show a large window (>0.6 V) between fully match cases and 1-bit mismatch cases of the 4-level CAM design, verifying its feasibility. The effects of 3D-NAND layers and parasitic resistance and capacitance on the properties of multi-level CAM design are also analyzed, which gives the guideline for improving process and material.

The research is published in the journal *Science China Information Sciences*.

More information: Haozhang Yang et al, An ultra-high-density and energy-efficient content addressable memory design based on 3D-NAND flash, *Science China Information Sciences* (2023). DOI: 10.1007/s11432-021-3502-4