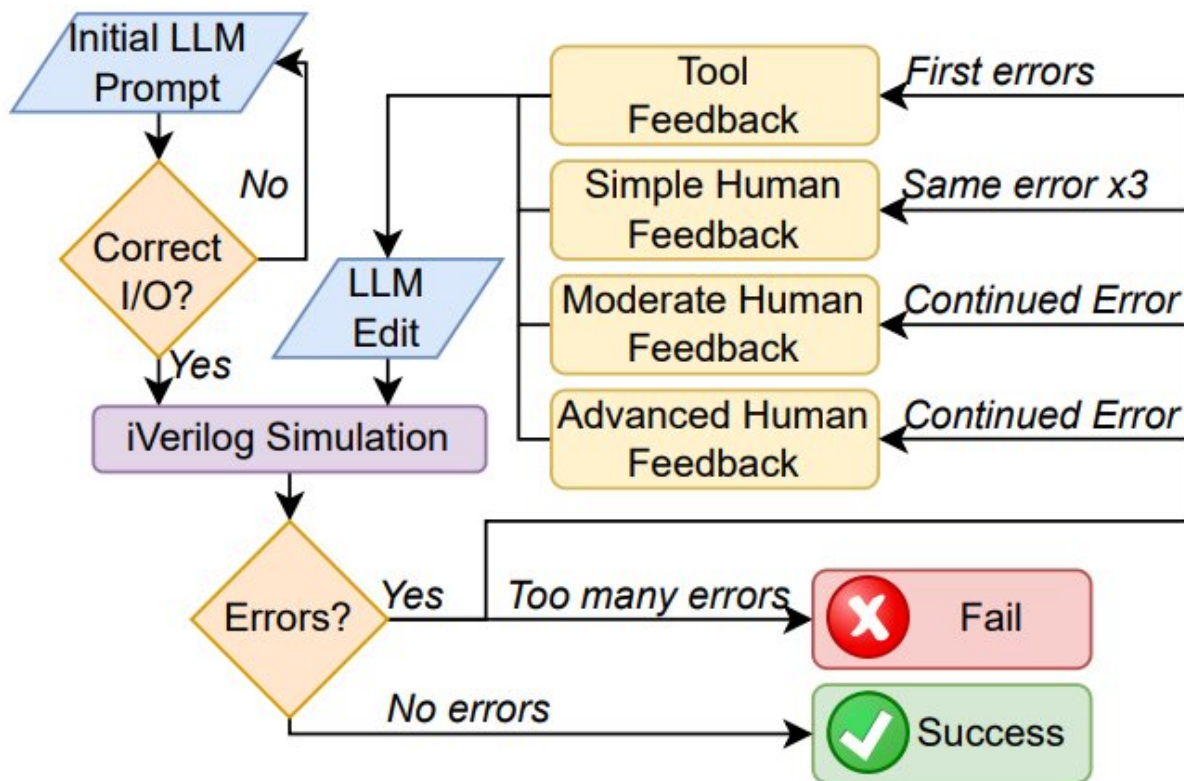


# Conversations with AI models can help create microprocessing chips, researchers discover

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Simplified LLM conversation flowchart. Credit: *arXiv* (2023). DOI: 10.48550/arxiv.2305.13243

Researchers at NYU Tandon School of Engineering have fabricated a microprocessing chip using plain English "conversations" with an AI

model, a first-of-its-kind achievement that could lead to faster chip development and allow individuals without specialized technical skills to design chips.

In a study posted to the *arXiv* pre-print repository, the research team presents how two [hardware](#) engineers "talked" in standard English with ChatGPT-4—a Large Language Model (LLM) built to understand and generate human-like text type—to design a new type of microprocessor architecture. The researchers then sent the designs to manufacture.

Typically, developing any type of hardware—including chips, the tiny electronic components that act as the brains of electronic devices—starts with describing what the hardware should do in normal language. Specially trained engineers then translate that description into Hardware Description Languages (HDLs), Verilog being one example, to create the actual circuit elements that allow the hardware to perform its tasks.

In this study, the LLM was able to produce workable Verilog through back-and-forth dialogue. The subsequent [chip](#) manufacture included the benchmarks and the processor, using a process called tapeout, in a Skywater 130nm shuttle, a specific kind of semiconductor manufacturing service, access to which was provided via Tiny Tapeout.

"This study resulted in what we believe is the first fully AI-generated HDL sent for fabrication into a physical chip," said NYU Tandon's Hammond Pearce, research assistant professor and a member of the research team. "Some AI models, like OpenAI's ChatGPT and Google's Bard, can generate software code in different programming languages, but their application in hardware design has not been extensively studied yet. This research shows AI can benefit hardware fabrication too, especially when it's used conversationally, where you can have a kind of back-and-forth to perfect the designs."

The NYU Tandon research team, which also includes Professor Ramesh Karri, Institute Associate Professor Siddharth Garg and doctoral student Jason Blocklove, used LLMs to work on eight hardware design examples, specifically by generating Verilog code for functional and verification purposes, before focusing on chip fabrication for a deep-dive case study. Previously, the researchers had tested LLMs to convert English to Verilog but, they said, adding back-and-forth interaction with a live engineer produced the best results.

According to the researchers, if implemented in real-world settings, using LLM conversations in chip fabrication could reduce [human error](#) in the HDL translation process, contribute to productivity gains, shorten design time and time to market and allow for more creative designs.

The process they developed could also eliminate the need for HDL fluency among chip designers, a relatively rare skill that represents a significant hurdle to people seeking those kinds of jobs.

Further testing is needed to identify and address security considerations involved in using AI for chip design, the researchers said.

With the federal CHIPS Act signed into law in August 2022, the United States is attempting to boost domestic research and manufacturing of semiconductor chips. According to the Semiconductor Industry Association, the U.S. currently accounts for only about 12% of the global semiconductor manufacturing capacity, and chip shortages during the COVID pandemic hampered availability of new cars and other chip-dependent devices.

**More information:** Jason Blocklove et al, Chip-Chat: Challenges and Opportunities in Conversational Hardware Design, *arXiv* (2023). [DOI: 10.48550/arxiv.2305.13243](https://doi.org/10.48550/arxiv.2305.13243)

Provided by NYU Tandon School of Engineering

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