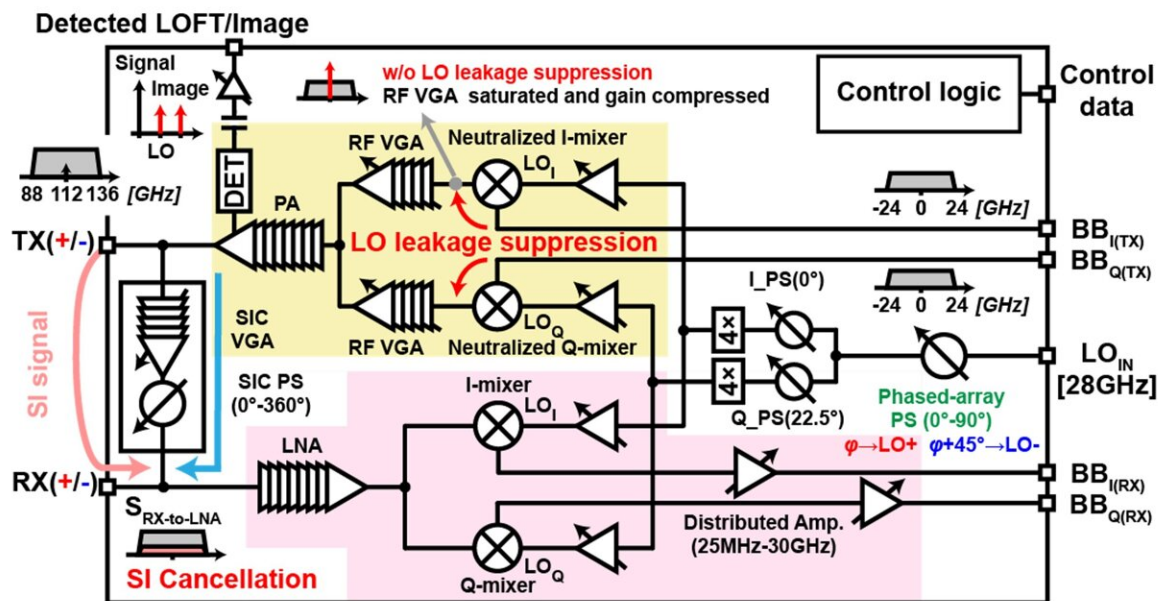


Preparing the stage for 6G: A fast and compact transceiver for sub-THz frequencies

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The proposed architecture focuses on minimizing self-interference (SI), the leakage of the transmitted signal (TX) into the receiver (RX). By adopting a symmetric antenna design and implementing a more precise self-interference cancellation (SIC) circuit, the system can reach unprecedented data rates at frequencies over 100 GHz. Credit: ©2023 VLSI Symposium

A new transceiver design capable of both transmission and reception at frequencies over 100 GHz and at 112 Gb/s data rate could pave the way

to 6G technologies, as reported by scientists at Tokyo Tech. By effectively suppressing the self-interference caused by the transmission signal leaking into the receiver, the proposed architecture reaches unprecedented data rates while maintaining a surprisingly compact size.

Scientists and engineers in the field of telecommunications are already working on the technologies that will be used for sixth generation (6G) networks. Ideally, 6G should deliver data rates of over 100 gigabits per second (Gb/s) and support extremely low latencies for applications such as autonomous cars and virtual reality. One way to meet these massive requirements for transmission and reception is to adopt a full-duplex (FD) architecture operating at sub-THz frequencies from 88 to 136 GHz.

The main advantage of the FD architecture is that it enables a single system to both transmit and receive signals, effectively doubling the throughput. One way to implement this architecture is to make the transmission and reception modules share a single antenna. This helps reduce the size of the circuit and allows both parts to make full use of the available frequency spectrum.

However, single-antenna FD architectures suffer greatly from self-interference (SI), a phenomenon in which the transmitted signal leaks into the receiver side. Such systems must include circuits for SI cancelation that attempt to cancel the generated SI by injecting an equal signal with the opposite polarity. In the sub-THz band, implementing effective SI cancelation is much more challenging than in [lower frequencies](#), which remains a hurdle to single-antenna FD designs.

Against this backdrop, a team of researchers from Tokyo Institute of Technology (Tokyo Tech), Japan, have recently developed a novel FD communication system addressing the obstacles posed by SI. The research team of Professor Kenichi Okada present their design at the the

2023 Symposium on VLSI Technology and Circuits held June 11-16, Kyoto, Japan.

One of the main features of their system is the implementation of a dual-polarized patch antenna. It is driven by differential signals—a combination of positive and negative feeding ports for transmission and reception. By making the circuit paths of these ports highly symmetrical, the mismatch of the transmitted signal that leaks into the differential receiver's ports is minimized, which helps keep SI low. "Our design avoids large transmission leakages prevalent in devices with asymmetric antenna structures and asymmetric differential signal ports," explains Prof. Okada.

Another important aspect of the proposed design is the SI cancellation (SIC) circuit. For effectively canceling the generated SI, one needs to carefully modify the phase of the cancellation signal such that it is opposite to that of the leaked signal. This is usually done using variable capacitors called varactors. However, at the sub-THz range, conventional varactors have a limited phase range and poor resolution. To tackle this problem, the researchers developed a new varactor structure that achieved excellent linear resolution over the entire sub-THz band and over the full 360° range.

The team tested their design through a series of experiments, which yielded quite promising results. "In the over-the-air measurement, the proposed FD transceiver achieved 6 Gb/s. The SI suppression was improved by 20 decibels when the SI canceler was turned on," says Prof. Okada.

The device, the world's first FD phased-array transceiver to operate at over 100 GHz, also achieved a data rate of 112 Gb/s in HD mode. This is the fastest-to-date system among sub-THz phased-array transceivers. Together with a compact size and a wide range of operating frequencies,

the proposed architecture represents a big step toward the telecommunications technology for 6G.

More information: A Sub-THz Full-Duplex Phased-Array Transceiver with Self-Interference Cancellation and LO Feedthrough Suppression, The 2023 Symposium on VLSI Technology and Circuits, www.vlsisymposium.org/index.html

Provided by Tokyo Institute of Technology

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