Developing a superior low-jitter CSS-ADPLL chip with a charge-steering sampling technique

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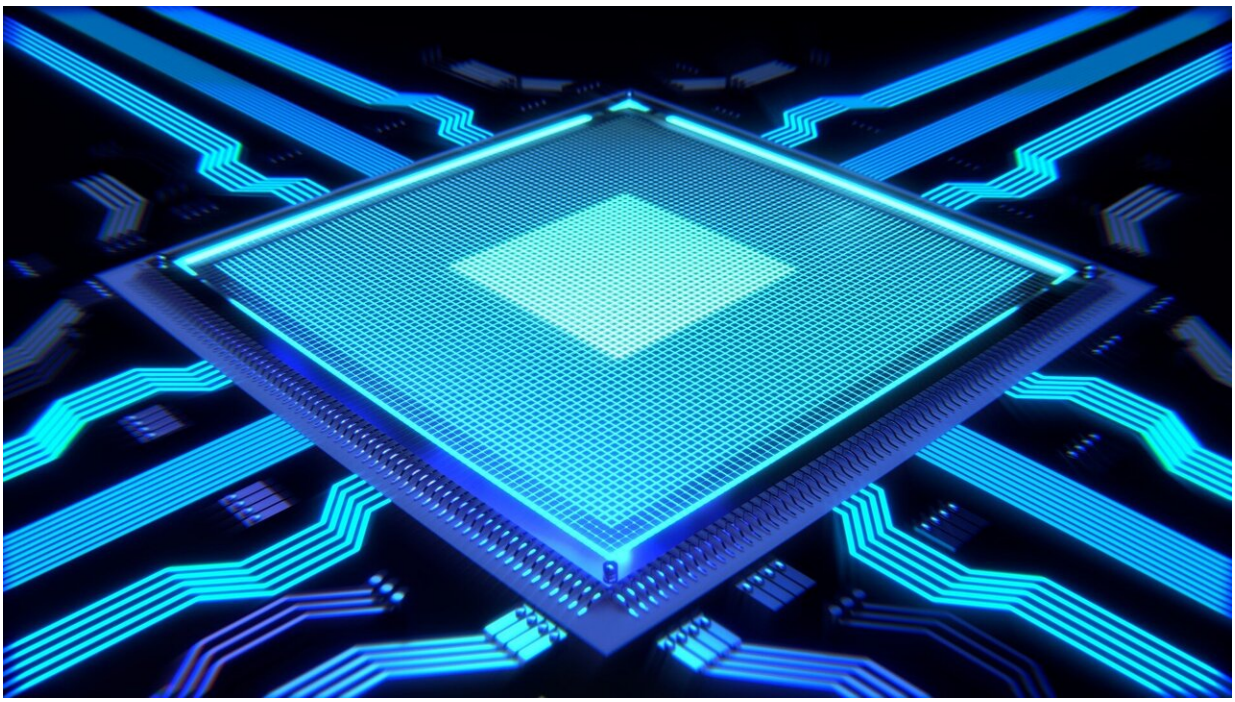

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A research team led by Prof. Hu Yizhe and Prof. Lin Fujiang from the University of Science and Technology of China (USTC) of the Chinese Academy of Sciences (CAS) designed a low-jitter millimeter-wave all-digital phase-locked loop (CSS-ADPLL) chip based on an innovative

charge-steering sampling (CSS) technique, which has been selected for participation in the 2023 Symposium on VLSI Technology and Circuits (VLSI Symposium).

As an international conference in the realm of large-scale integrated circuit chip design and process technology, the VLSI Symposium provides an influential platform for showcasing the latest advancements in IC technology. This year, the event took place in Kyoto, Japan, from June 11 to 16. The selection of the CSS-ADPLL chip underscores its technological superiority, derived from the cutting-edge charge-steering sampling (CSS) technique, particularly in achieving ultra-low jitter performance for millimeter-wave applications.

The low-jitter millimeter-wave frequency synthesizer chip, which serves as a vital component in enabling 5G/6G millimeter-wave communications, delivers precise carrier signals for millimeter-wave communication systems. In this study, the research team combined charge-steering sampling with a successive approximation register-type analog-to-digital converter (SAR-ADC) using the charge rudder sampling technique.

This approach enabled the construction of a digital phase discriminator with exceptional phase-identification gain, high linearity, and multi-bit digital outputs.

The CSS-ADPLL chip boasts a compact structure, comprising a charge rudder discriminator (CSS-PD), a SAR-ADC, a digital filter, and a digital filter. Furthermore, it incorporates an ADC, digital filter, and numerically controlled oscillator, all contributing to excellent phase noise performance, fast locking speed, and minimal power consumption.

The test results demonstrate that the chip has achieved a clock jitter of 75.9 fs, a reference spurious level of -50.13 dBc, and an outstanding

Figure of Merit (FoM) value of -252.4 dB. These results establish it as the leading performer among digital phase-locked loops operating above 20 GHz. The chip's core area measures just 0.044 mm^2.

The research findings were presented at the conference under the title "An 18.8-to-23.3 GHz ADPLL Based on Charge-Steering-Sampling Technique Achieving 75.9 fs RMS Jitter and -252 dB FoM."

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