Novel lateral data storage: Two-dimensional ferroelectric semiconductor memory

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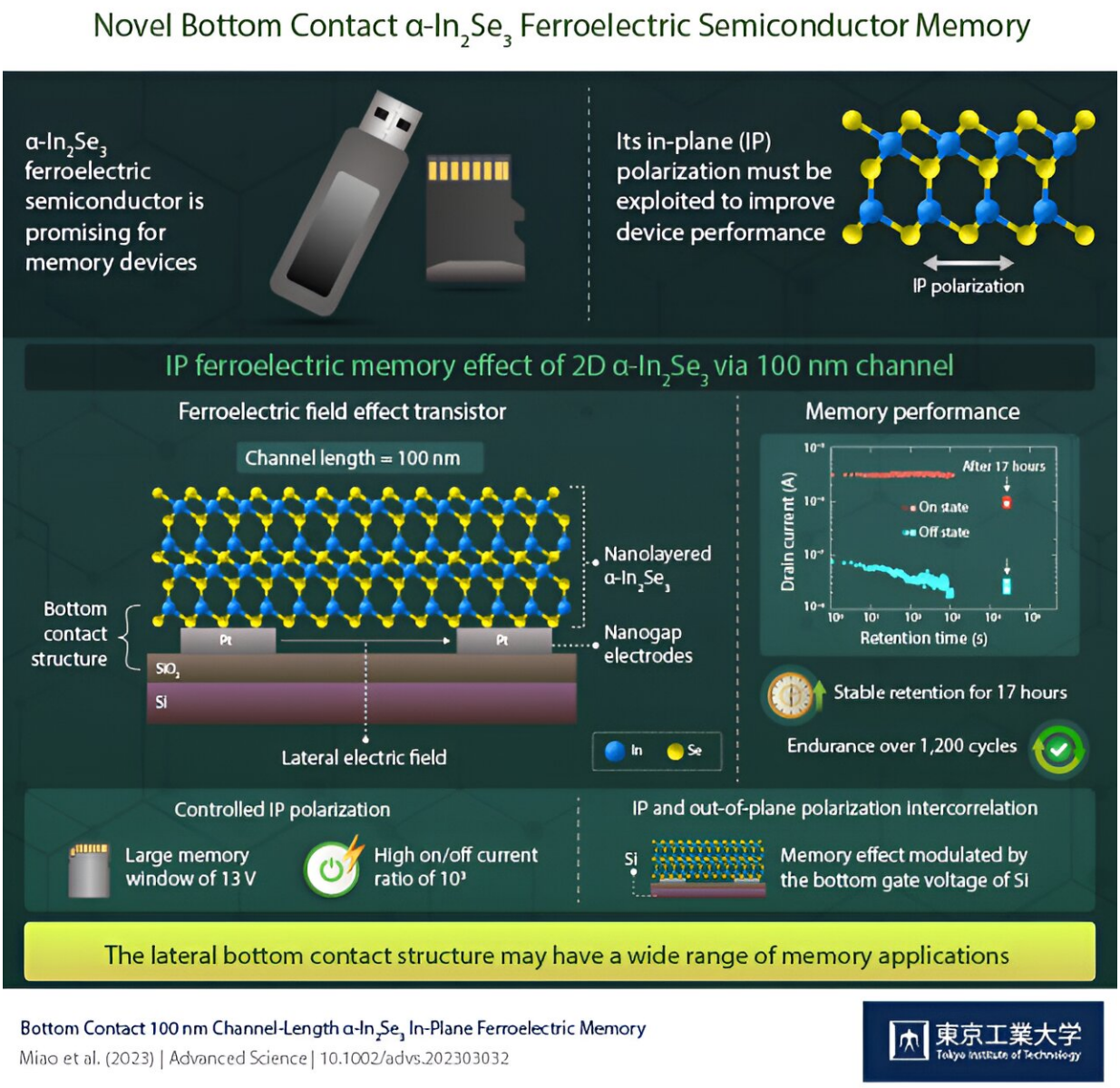

Bottom Contact 100 nm Channel-Length α-In_2Se_3 In-Plane Ferroelectric Memory

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The lateral bottom contact structure may have a wide range of memory applications. Credit: Tokyo Tech

Traditional memory technologies face limitations in terms of speed, scalability, and power consumption, making them unsuitable for future data-intensive applications. Ferroelectric memory has garnered immense interest in recent years due to its potential for non-volatile storage, enabling data retention even when the power is turned off. The development of two-dimensional (2D) van der Waals material α-In_2Se_3 has also opened new opportunities for advancing memory technologies.

Interestingly, ferroelectric memory takes a giant step forward by incorporating the remarkable properties of α-In_2Se_3. It is renowned for high carrier mobility, tunable bandgap, and strong ferroelectric properties at the atomic level, making it ideal for high-speed memory applications.

However, the scope of research is limited by the lack of lateral α-In_2Se_3 devices that demonstrate in-plane (IP) polarization-controlled electrical characteristics. When fabricating bottom-contact ferroelectric field-effect transistors by 2D material exfoliation, wide electrode width is preferred to improve the overall yield.

However, achieving nanoscale channel lengths for the nanogap electrodes becomes challenging when simultaneously employing wide electrode widths, mainly due to the substantial ratio between the electrode width and channel length.

Recently, a team of researchers led by Professor Yutaka Majima from Tokyo Institute of Technology (Tokyo Tech) proposed a new concept of bottom contact structure at the nano level to solve this problem. They

have designed a ferroelectric semiconductor memory device with a two-terminal nanogap-structured bottom contact by leveraging the IP polarization flipping of α-In_2Se_3. Their work is published in *Advanced Science*.

Distinct from previous devices, α-In_2Se_3 is exfoliated on electrodes as the bottom contact in the present design. The IP polarization can be reversed by applying a drain voltage via a channel with a relatively narrow length of 100 nm. This lateral channel design allows for higher memory density, enabling the integration of many memory cells on a single chip.

Furthermore, the lateral memory configuration employed in the proposed technology enables seamless integration with existing semiconductor device fabrication techniques, facilitating a smooth transition from current memory technologies to non-volatile ferroelectric memory.

The researchers found that the α-In_2Se_3 ferroelectric memory exhibits typical resistive switching, a high on/off ratio of over 10^3, a large memory window of 13 V, good retention for 17 hours, and endurance for 1,200 cycles. This will pave the way for non-volatile ferroelectric memory. Notably, massive integration becomes promising with a bottom contact structure, considering the simplified construction of next-generation electronics.

"Our ferroelectric semiconductor memory cultivates the IP polarization α-In_2Se_3 from a 100 nm bottom contact design, representing a significant leap forward in memory technology," says Prof. Majima. "We believe that this design will pave the way in which data is stored and accessed and open up exciting opportunities for various applications, including artificial intelligence, edge computing, and Internet of Things devices."

More information: Shurong Miao et al, Bottom Contact 100 nm Channel-Length α-In2Se3 In-Plane Ferroelectric Memory, *Advanced Science* (2023). DOI: 10.1002/advs.202303032

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