Chip design with machine learning: A survey from an algorithm perspective

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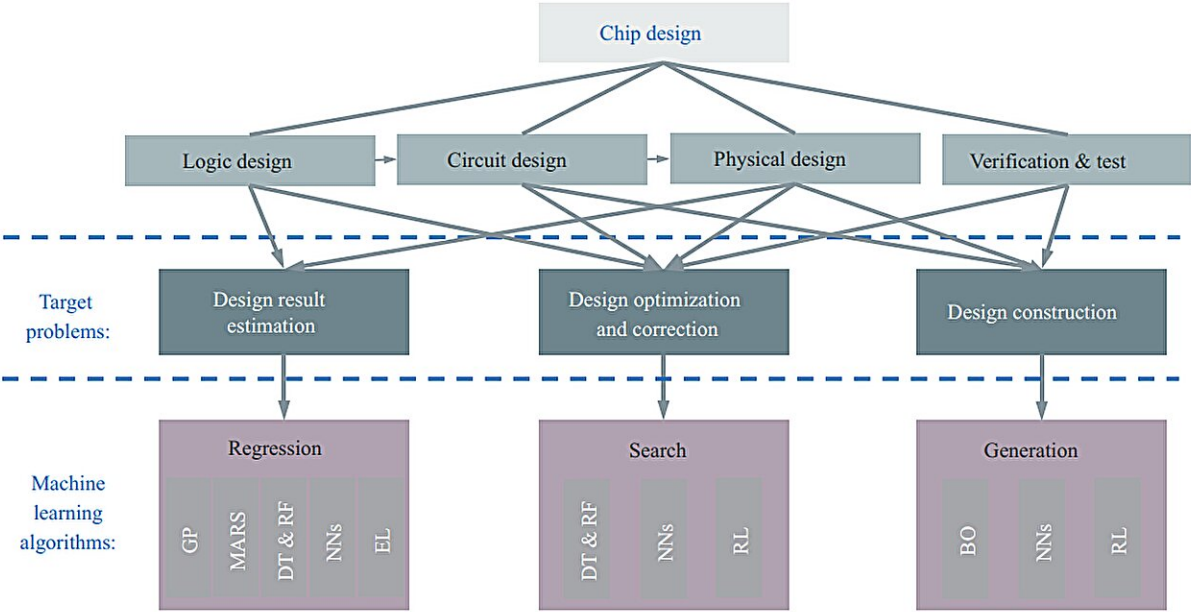

Figure 1   (Color online) Overall taxonomy.

Overall taxonomy. Credit: Science China Press

A paper published in the journal *Science China Information Sciences* comprehensively surveys existing works of chip design with ML algorithms from an algorithm perspective. To accomplish this goal, the authors propose a novel and systematical taxonomy for the target problems at different stages in chip design. The taxonomy aims to guide selecting and designing ML algorithms for the target problems, taking

into account their existing challenges, as well as to provide a comprehensive summary of chip design with ML algorithms for researchers.

The authors classify the target problems in chip design into three categories: Design Result Estimation, Design Optimization and Correction, and Design Construction, which are commonly encountered in different stages of logic design, circuit design, and physical design, as well as in verification and test of each stage.

Specifically, design result estimation encompasses problems that predict or estimate design quality, such as performance estimation in logic design, IR drop estimation in physical design, and Static Timing Analysis (STA) in logic design and physical design. Design optimization and correction refer to problems that optimize design quality and correct design errors, respectively, such as HLS Design Space Exploration (DSE) in logic design, logic optimization in circuit design, and detailed routing in physical design.

Design construction encompasses problems that generate design representations or add the design objects (i.e., components and routes), such as physical mapping in circuit design and global placement in physical design.

To address these target problems with ML algorithms, the authors formulate the three categories of the target problems as three corresponding problems in ML: regression, search, and generation.

Each of these ML problems can be tackled by various ML algorithms. Specifically, the design result estimation problem is formulated as a regression problem and can be addressed using several ML algorithms, including Gaussian Process (GP), Multivariate Adaptive Regression Splines (MARS), Decision Tree (DT) & Random Forest (RF), Neural

Networks (NNs), and Ensemble Learning (EL).

The design optimization and correction problem is formulated as a search problem and can be tackled using various ML algorithms, including DT & RF, NNs, and RL. Finally, the design construction problem is formulated as a generation problem and can be tackled using various ML algorithms, including Bayesian Optimization (BO), NNs, and RL.

Based on the taxonomy, the authors comprehensively survey the existing works in terms of the target problems by the following steps. Their approach is structured as follows: firstly, they present a definition for each target problem and analyze the inherent reasons for applying ML algorithms in addressing these target problems.

Secondly, they conduct a comprehensive survey in terms of target problems according to the ML algorithms. They introduce specific ML-based works for each target problem and explain how they improve upon the origin chip design tools based on conventional algorithms.

Finally, they conclude by highlighting three key challenges that remain unresolved in the existing works and provide several insights for future research in chip design with ML algorithms, including single-stage end-to-end generation, cross-stage end-to-end generation, whole-process end-to-end generation, practicability improvement, and others, which the authors hope to boost the research in chip design with ML.

By establishing a clear link between chip design problems and corresponding ML solutions, the survey aims to shed light on the road to chip design intelligence from previous chip design automation.

To the best of the authors' knowledge, this paper is the first work to comprehensively survey chip design with ML from an [algorithm](#)

perspective. The authors summarize the main contributions of this survey as follows:

1. Deep analysis of chip design. The authors dissect the commonly adopted process of chip design and analyze the key steps in different design stages (i.e., logic design, circuit design, and physical design) as well as in verification and test of each stage, where the key design, advantages, and disadvantages of the steps are analyzed.
2. Innovative taxonomy. The authors classify target problems into three categories (i.e., design result estimation, design optimization and correction, and design correction) and further formulate them into three ML problems, respectively: regression, search, and generation.
3. Comprehensive survey. Based on the taxonomy, the authors present the definition of each target problem and analyze the inherent reasons why ML algorithms are used to address the target problems. The authors also conduct a comprehensive survey in terms of target problems based on different ML algorithms.
4. Future works. Finally, the authors conclude by highlighting three key challenges that remain unsolved in existing works and provide insights into the future development of chip design with ML algorithms, which the authors hope to boost the research in chip design with ML.