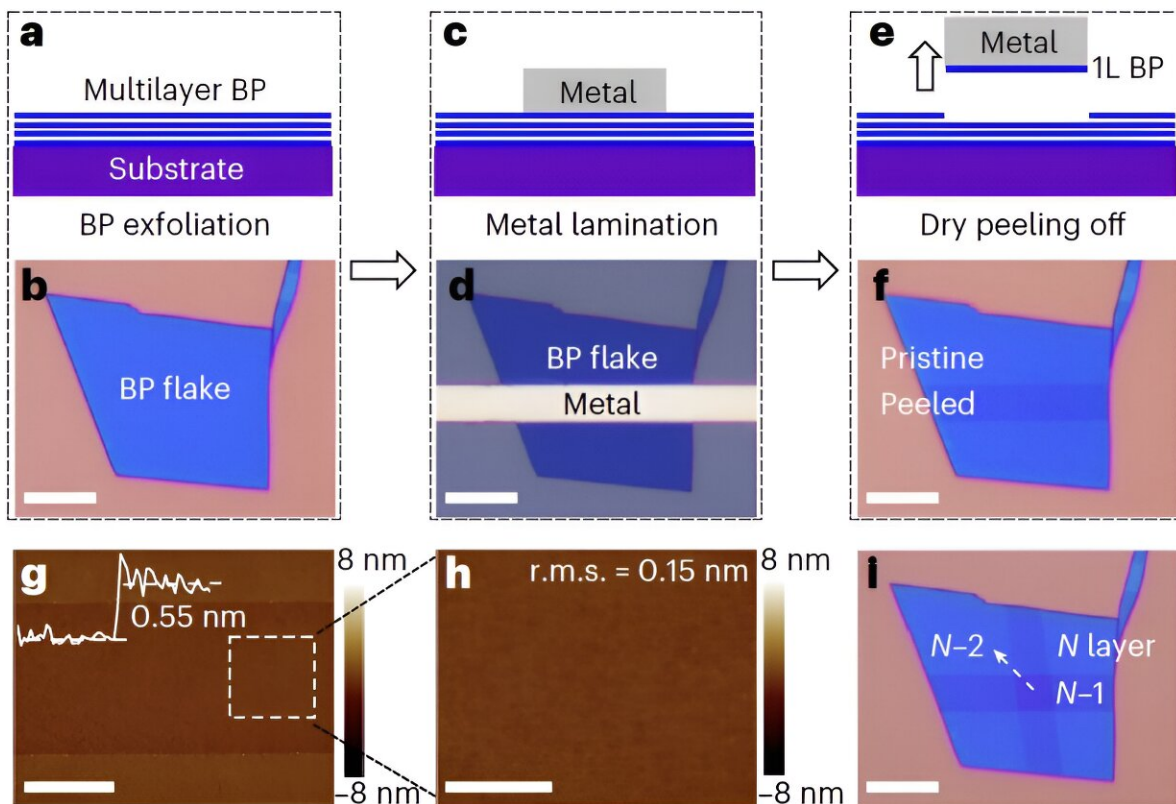


New transistors based on monolayer black phosphorus and germanium arsenide

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Fabrication processes for vdW peeling of BP. a,b, Schematic (a) and optical image (b) of a multilayer BP flake exfoliated onto a silicon substrate. c,d, Schematic (c) and optical image (d) of a Pt stripe physically laminated on top of a BP flake. e,f, By physically peeling off the Pt stripe (e), the topmost BP layer is dry-removed and the intrinsic properties of the remaining layers are retained (f). 1L, one layer. g,h, AFM height measurement (g) and zoomed-in AFM image (h) for the vdW peeled BP flake shown in f. The thinned region demonstrates a

small surface roughness (root-mean-square, r.m.s.) of 0.15 nm, indicating the pristine surface after the vdW peeling process. i, Optical image of the second peeling of the BP flake shown in f, with 90° rotation of the Pt stripe. Scale bars, 10 μm in b, d, f and i, 3 μm in g and 1 μm in h. Credit: *Nature Electronics* (2023). DOI: 10.1038/s41928-023-01087-8

Two-dimensional (2D) semiconducting materials have proved to be very promising for the development of various electronic devices, including wearables and smaller electronics. These materials can have significant advantages over their bulky counterparts, for instance retaining their carrier mobility irrespective of their reduced thickness.

Despite their promise for creating thin electronics, 2D semiconductors have so far only rarely been used to create monolayer transistors, thinner versions of the crucial electronic components used to modulate and amplify electrical current inside most existing devices. Most proposed monolayer transistors based on 2D semiconductors were created using a few carefully selected materials known to have relatively stable lattice structures, such as graphene, tungsten diselenide or molybdenum disulfide (MoS₂).

Researchers at Hunan University, the Chinese Academy of Sciences and Wuhan University recently set out to develop new monolayer transistors using alternative 2D semiconducting materials that have so far been primarily used to create multi-layer transistors, including black phosphorus (BP) and germanium arsenide (GeAs). Their work is [published](#) in the journal *Nature Electronics*.

"For a number of promising 2D materials—such as black phosphorus and germanium arsenide—the fabrication of monolayer transistors is challenging and is limited by the difficulties in forming robust electrical

contacts with the delicate 2D materials," Wangying Li, Quanyang Tao and their colleagues wrote in their paper. "We report the fabrication of monolayer black phosphorus and germanium arsenide transistors with three-dimensional raised contacts using a van der Waals peeling technique."

The primary objective of the recent work by this team of researchers was to create new transistors based on monolayer 2D semiconductors beyond those that have so far been primarily used in monolayer transistor designs. This presents several challenges, as some of these materials are difficult to scale down uniformly and without compromising their intrinsic properties.

To achieve this, Li, Tao and their collaborators devised a van der Waals (vdW) peeling technique that can be used to create monolayer 2D transistors with 3D raised contacts. This technique entails laminating flat metals onto multilayer 2D channels, which in turn allows the researchers to remove the semiconducting layer at the top of the stack by peeling off the metal.

"Through layer-by-layer mechanical peeling, the channel region of a multilayer black phosphorus transistor can be gradually reduced to monolayer thickness without degrading its delicate lattice and while retaining a multilayer contact region," Li, Tao and their colleagues wrote.

As part of their study, the team used their proposed peeling technique to create homo-junctions and homo-superlattices based on various 2D semiconductors, including BP, GeAs, InSe (indium selenide) and GaSe (gallium selenide).

The team found that their proposed method allowed them to thin down the channel part of their transistors while maintaining the required

thickness in the contact region.

"Using the technique, we measure the [electrical properties](#) of the same 2D transistor with different channel thicknesses," Li, Tao and their colleagues wrote. "We find that the carrier mobility of [black phosphorus](#) drops sharply when reducing body thickness, behaving more like a conventional bulk [semiconductor](#) rather than a pure van der Waals semiconductor."

As part of their recent study, the researchers demonstrated the potential of their technique for developing promising monolayer transistors with 3D-raised contacts based on BP and GeAs. In the future, their layer-by-layer peeling method could open new horizons for the creation of thinner and scalable transistors using uncommon 2D semiconductors that are typically viewed as poorly performing for these applications.

"The work has potential implications for other unstable [monolayer](#) materials beyond 2D semiconductors such as organic monolayers and perovskite monolayers, which have previously been considered to be non-conductive or to have poor intrinsic properties, but which are actually limited by the poor contact between the metal and monolayers," Li, Tao and their colleagues added.

More information: Wanying Li et al, Monolayer black phosphorus and germanium arsenide transistors via van der Waals channel thinning, *Nature Electronics* (2023). [DOI: 10.1038/s41928-023-01087-8](https://doi.org/10.1038/s41928-023-01087-8)

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