Combating fractional spurs in phase locked loops to improve wireless system performance in beyond 5G

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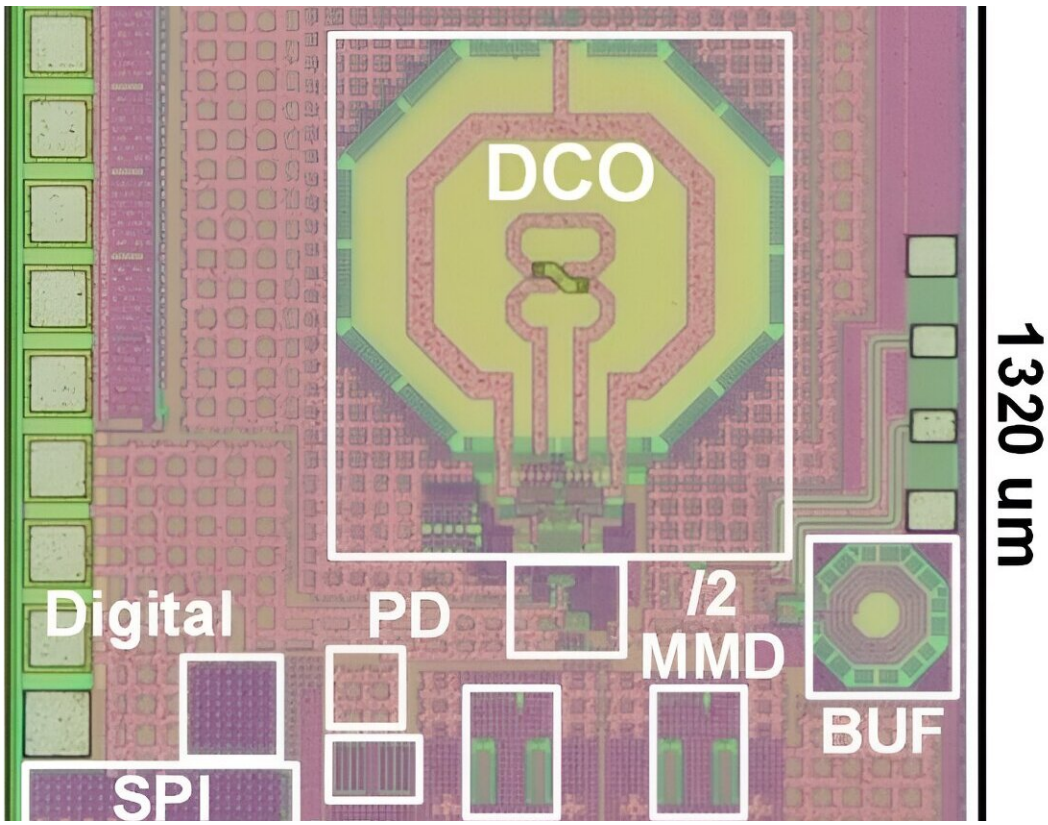


The total power consumption of the proposed PLL is only 8.89 mW from a 1 V supply, which leads to a figure of merit of reference of -247.4 dB. Credit: ISSCC 2024

Two innovative design techniques lead to substantial improvements in performance in fractional-N phase locked loops (PLLs), report scientists from Tokyo Tech.

The proposed methods aim to minimize unwanted signals known as fractional spurs, which typically plague PLLs used in many modern radar systems and wireless transceivers. These efforts could open doors to technological improvements in wireless communication, autonomous vehicles, surveillance, and tracking systems in beyond 5G era.

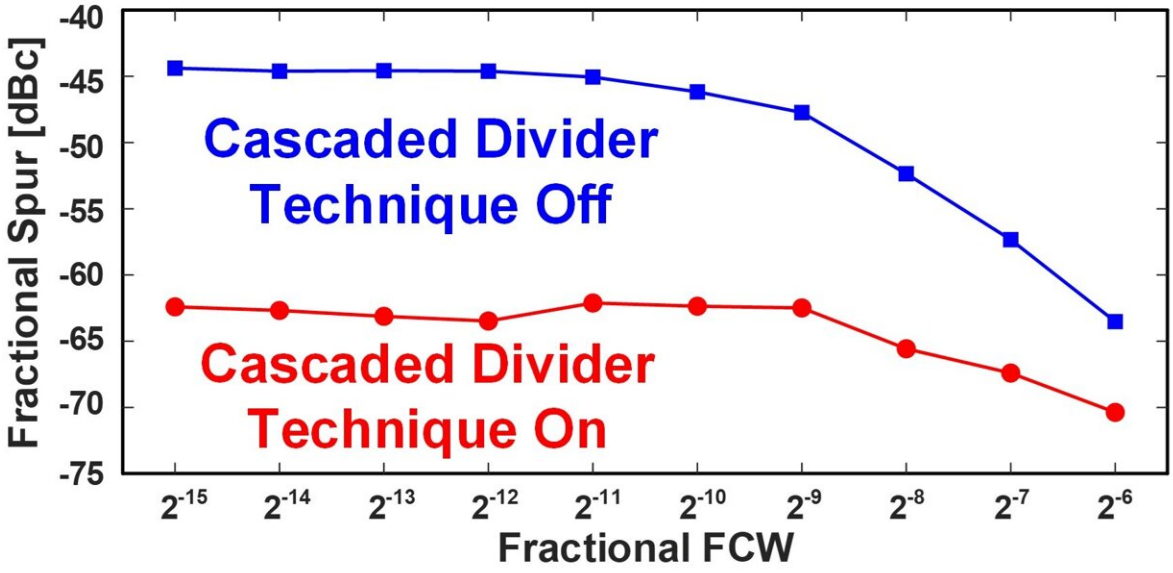
Many emerging and evolving technologies, such as self-driving vehicles, target tracking systems, and remote sensors, rely on the high-speed and error-free operation of wireless data transceivers and radar systems. In these applications, phase locked loops (PLLs) are crucial components that help with the synthesis, modulation, and synchronization of oscillating signals. Thus, eliminating or minimizing sources of error in PLLs is essential to improve the overall performance of systems.

In fractional-N PLLs, a popular type of PLL with excellent resolution and flexible control of frequency, jitter and fractional spurs are mainstay enemies. "Jitter" refers to the overall deviation from the ideal timing of the synthesized oscillation. On the other hand, fractional spurs are unwanted signals that arise from the periodicity in the error.

Components called digital-to-time converters (DTCs) are typically used in the digital PLLs to cancel the quantization error, but imperfections in DTCs due to so-called "integral non-linearities (INLs)" ultimately manifest as fractional spurs that degrade phase noise in the output of the PLL.

A research team from Tokyo Institute of Technology (Tokyo Tech), led by Professor Kenichi Okada, sought to address these problems through the development of two innovative design techniques leading to a low-

spur fractional-N PLL. Their work has been published in the *Proceeding of the 2024 IEEE International Solid-State Circuits Conference (ISSCC)*.



The proposed cascaded divider technique achieves a substantially improved PLL performance by minimizing fractional spurs. Credit: ISSCC 2024

The first proposed technique involves the use of a cascaded-fractional divider. This method involves splitting the frequency control word (FCW), an internal PLL signal that controls the output frequency, into two but in a way that both are far from an integer value.

The logic underlying this is that for far-integer FCWs, fractional spurs appear in the PLL in higher frequencies, and high-frequency components are naturally filtered out by the inherent operations of the PLL. Notably, this approach does not involve digital pre-distortion (DPD), a technique that introduces complexity and causes slower phase locking.

The second proposed technique revolves around a pseudo-differential DTC to avoid the pitfalls of standard DTC implementations.

"In conventional DTC designs, there are stringent trade-offs between the DTC power, delay range, noise, and INL, limiting the minimum fractional-spur level achievable," explains Prof. Okada. To tackle this issue, the researchers noted that the non-linearities of DTCs contain even symmetric components. Accordingly, they implemented the function of a single DTC using two half-range DTCs with the same even-symmetric INLs in differential operation. As a result, these INLs were naturally canceled out via subtraction at the PLL's phase detector.

The team tested their ideas by implementing the proposed digital PLL using a 65 nm CMOS process, requiring an active circuit area of only 0.23 mm^2. By comparing the performance of their device with other state-of-the-art designs, the researchers noted several advantages.

"By suppressing fractional spurs, the integrated PLL jitter was reduced from 243.5 fs to 143.7 fs," says Prof. Okada. "Thanks to the proposed cascaded fractional divider and pseudo-differential DTC techniques, we achieved the lowest class of jitter without DPD technology."

This innovative design may lead to technological improvements across many applications where fractional-N PLLs are a mainstay.

More information: A 7GHz Digital PLL with Cascaded Fractional Divider and Pseudo-Differential DTC Achieving -62.1dBc Fractional Spur and 143.7fs Integrated Jitter, *Proceeding of the 2024 IEEE International Solid-State Circuits Conference (ISSCC)*

Provided by Tokyo Institute of Technology