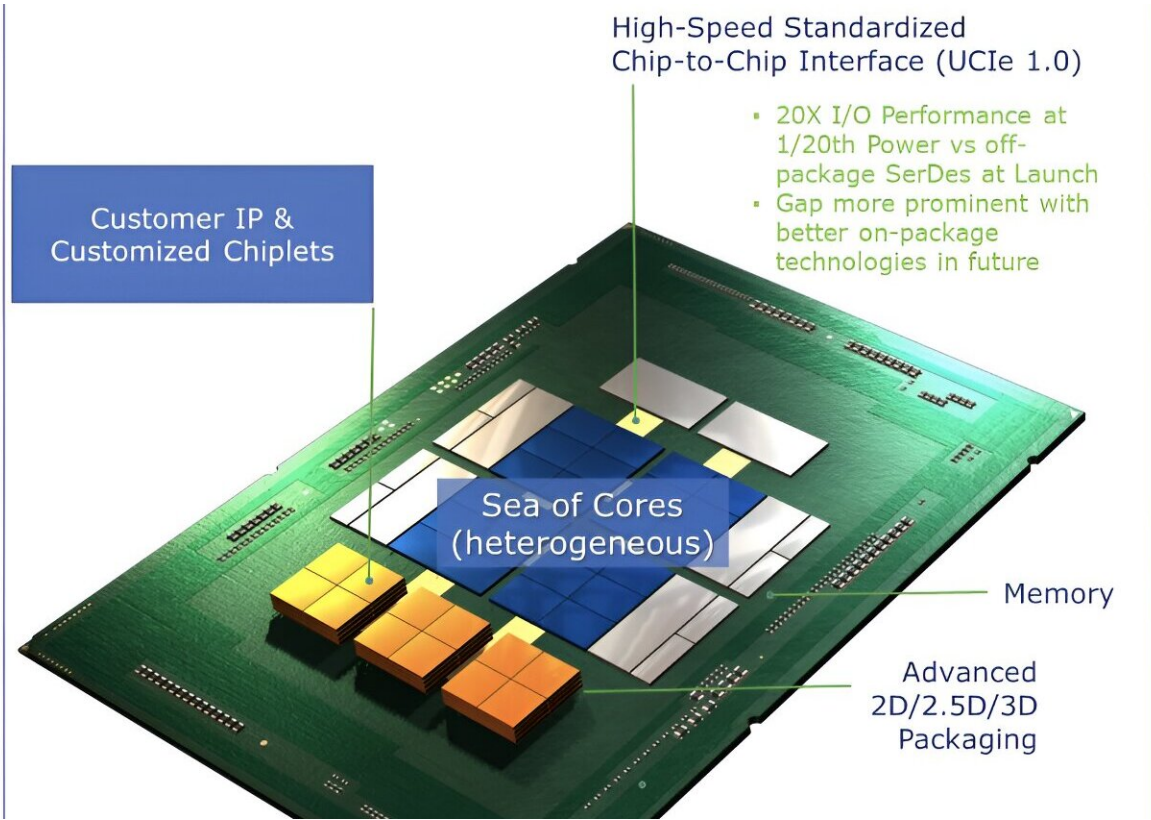


Intel introduces approach to boost power efficiency, reliability of packaged chiplet ecosystems

March 13 2024, by Ingrid Fadelli



Credit: Das Sharma et al

The integration of electronic chips in commercial devices has significantly evolved over the past decades, with engineers devising

various integration strategies and solutions. Initially, computers contained a central processor or central processing unit (CPU), connected to memory units and other components via traditional communication pathways, known as front-side-bus (FSB) interfaces.

Technological advances, however, have enabled the development of new integrated circuit (IC) architectures relying on multiple chiplets and more sophisticated electronic components. Intel Corporation played a crucial role in these developments, by introducing new architectures and specifications for the design of systems with multiple packaged chiplets.

Researchers at Intel Corporation Santa Clara recently outlined a new vision for further boosting the performance of systems developed following universal chiplet interconnect express (UCIe), a specification to standardize the connections between multi-function chiplets in modern System-in-Package (SiP). Their proposed approach, presented in a [paper](#) in *Nature Electronics*, entails reducing the frequency in these circuits to boost their power efficiency and performance.

"We have been driving technologies, such as PCI-Express, CXL, and UCIe, that are multi-generational," Dr. Debendra Das Sharma, Intel Senior Fellow and co-GM of Memory and I/O Technologies, Data Platforms and Artificial Intelligence Group at Intel Corporation, told Tech Xplore. "In the context of UCIe, after completing UCIe 1.0, we have been looking at how to deliver another order or two more performance with ideally an order lower power per bit to meet the insatiable demand for power-efficient performance."

Advances in the development of silicon and packaging technology have opened new possibilities for reducing the spacing between the bumps that connect individual chips within circuit boards, also known as bump pitches. The primary objective of the study by Dr. Das Sharma and his collaborators was to explore strategies that would allow researchers to

further boost the performance and power efficiency of systems as these bump pitches continue to be reduced for on-package interconnects.

"The trend in advanced packaging, including 3D, is reduced bump pitch," Dr. Das Sharma said. "Bump pitch is the minimum distance between two bumps that will connect two chiplets. So, that means we get more wires between two chiplets as the bump pitch reduces. The natural tendency, primarily borne out of external interconnects, is to push the frequency higher. However, in this case, since the number of wires increases, we need to push the frequency lower to make the circuits fit and get lower power."

As part of their study, Dr. Das Sharma and his colleagues carried out analyses to further explore the effects of reducing the frequency in systems based on packaged chiplets. They found that contrary to traditional chip connectivity interfaces, UCIe-aligned technologies significantly benefitted from a reduction in frequency as bump interconnect pitches were reduced.

Specifically, reductions in frequency were found to improve both the systems' power efficiency and their overall performance. Overall, this recent paper thus identifies a new valuable approach that could contribute to the future advancements of systems with interconnected circuits as their underlying architecture evolves further.

"We hope that the broad industry can benefit from our work through standardization the same way we have done in the past influencing industry standard specifications," Dr. Das Sharma added. "Personally, I now plan to continue to work to evolve industry standard interconnects like UCIe, CXL, PCIe as I have done for more than two decades. In the context of chiplets and UCIe, the journey has just started and I am excited about the opportunities ahead of us."

More information: Debendra Das Sharma et al, High-performance, power-efficient three-dimensional system-in-package designs with universal chiplet interconnect express, *Nature Electronics* (2024). [DOI: 10.1038/s41928-024-01126-y](https://doi.org/10.1038/s41928-024-01126-y)

© 2024 Science X Network

Citation: Intel introduces approach to boost power efficiency, reliability of packaged chiplet ecosystems (2024, March 13) retrieved 27 April 2024 from <https://techxplore.com/news/2024-03-intel-approach-boost-power-efficiency.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.