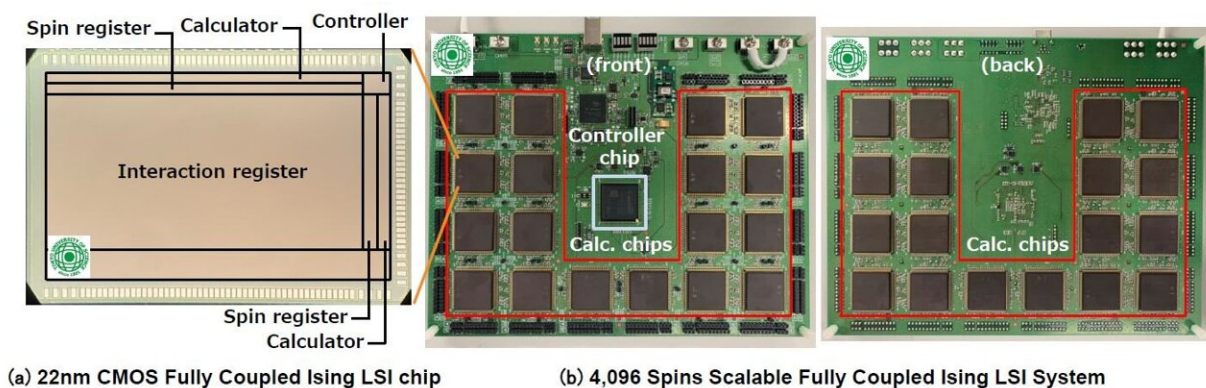


Semiconductors at scale: New processor achieves remarkable speedup in problem solving

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(a) The die photo of a 22nm fully-coupled Ising LSI chip; (b) the front and back views of the board of a 4096-spin scalable full-coupled Ising LSI system. Credit: Takayuki Kawahara from TUS

Annealing processors are designed specifically for addressing combinatorial optimization problems, where the task is to find the best solution from a finite set of possibilities. This holds implications for practical applications in logistics, resource allocation, and the discovery of drugs and materials.

In the context of CMOS (a type of semiconductor technology), it is necessary for the components of annealing processors to be fully

"coupled." However, the complexity of this coupling directly affects the scalability of the processors.

In a new *IEEE Access* [study](#) led by Professor Takayuki Kawahara from Tokyo University of Science, researchers have developed and successfully tested a scalable processor that divides the calculation into multiple LSI chips. The innovation was also presented in [IEEE 22nd World Symposium on Applied Machine Intelligence and Informatics \(SAMI 2024\)](#) on 25 January 2024.

According to Prof. Kawahara, "We want to achieve advanced information processing directly at the edge, rather than in the cloud or performing preprocessing at the edge for the cloud. Using the unique processing architecture announced by the Tokyo University of Science in 2020, we have realized a fully coupled LSI (Large Scale Integration) on one chip using 28nm CMOS technology. Furthermore, we devised a scalable method with parallel-operating chips and demonstrated its feasibility using FPGAs (Field-Programmable Gate Arrays) in 2022."

The team created a scalable annealing processor. It used 36 22nm CMOS calculation LSI (Large Scale Integration) chips and one control FPGA. This technology enables the construction of large-scale, fully coupled semiconductor systems following the Ising model (a mathematical model of magnetic systems) with 4096 spins.

The processor incorporates two distinct technologies developed at the Tokyo University of Science. This includes a "spin thread method" that enables 8 parallel solution searches, coupled with a technique that reduces chip requirements by about half compared to conventional methods. Its power needs are also modest, operating at 10MHz with a [power consumption](#) of 2.9W (1.3W for the core part). This was practically confirmed using a vertex cover problem with 4096 vertices.

In terms of power performance ratio, the processor outperformed simulating a fully coupled Ising system on a PC (i7, 3.6GHz) using annealing emulation by 2,306 times. Additionally, it surpassed the core CPU and arithmetic chip by 2,186 times.

The successful machine verification of this processor suggests the possibility of enhanced capacity. According to Prof. Kawahara, who holds a vision for the social implementation of this technology (such as initiating a business, joint research, and [technology transfer](#)), "In the future, we will develop this technology for a joint research effort targeting an LSI system with the computing power of a 2050-level quantum computer for solving combinatorial optimization problems."

"The goal is to achieve this without the need for [air conditioning](#), large equipment, or cloud infrastructure using current semiconductor processes. Specifically, we would like to achieve 2M (million) spins by 2030 and explore the creation of new digital industries using this."

In summary, researchers have developed a scalable, fully coupled annealing [processor](#) incorporating 4096 spins on a single board with 36 CMOS chips. Key innovations, including chip reduction and parallel operations for simultaneous solution searches, played a crucial role in this development.

More information: Taichi Megumi et al, Scalable Fully-Coupled Annealing Processing System Implementing 4096 Spins Using 22nm CMOS LSI, *IEEE Access* (2024). [DOI: 10.1109/ACCESS.2024.3360034](https://doi.org/10.1109/ACCESS.2024.3360034)

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