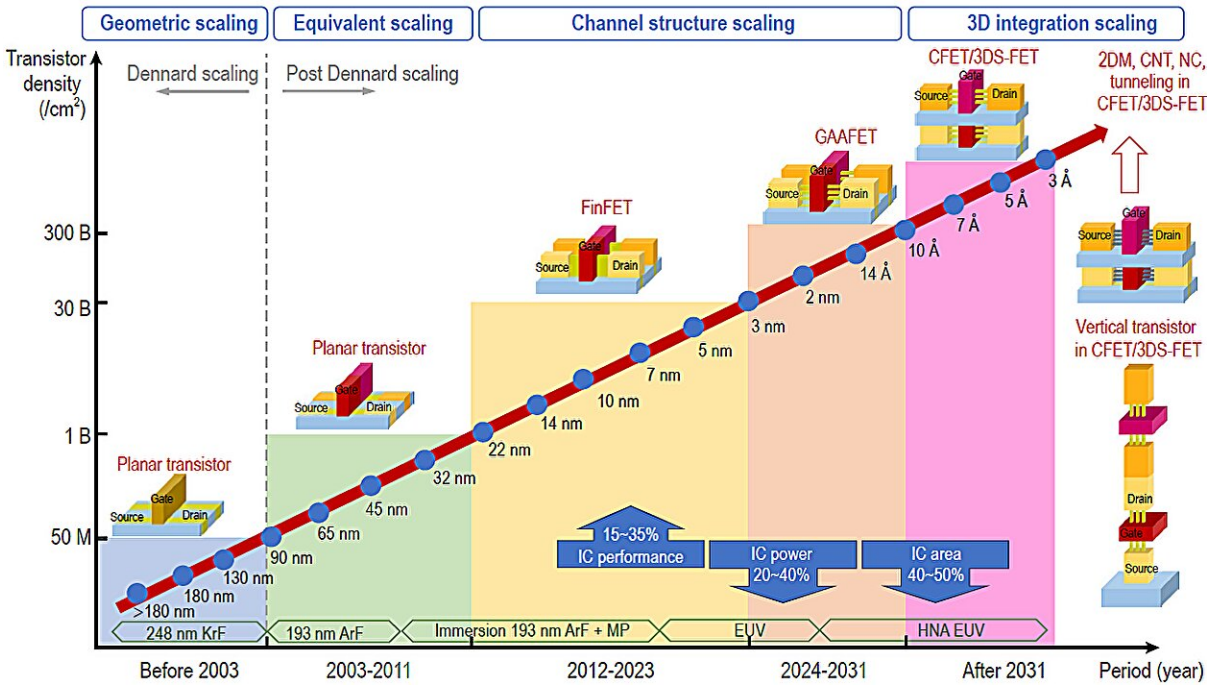


# New structure transistors for advanced technology node CMOS ICs

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CNT, or AOS materials for the future. Credit: Science China Press

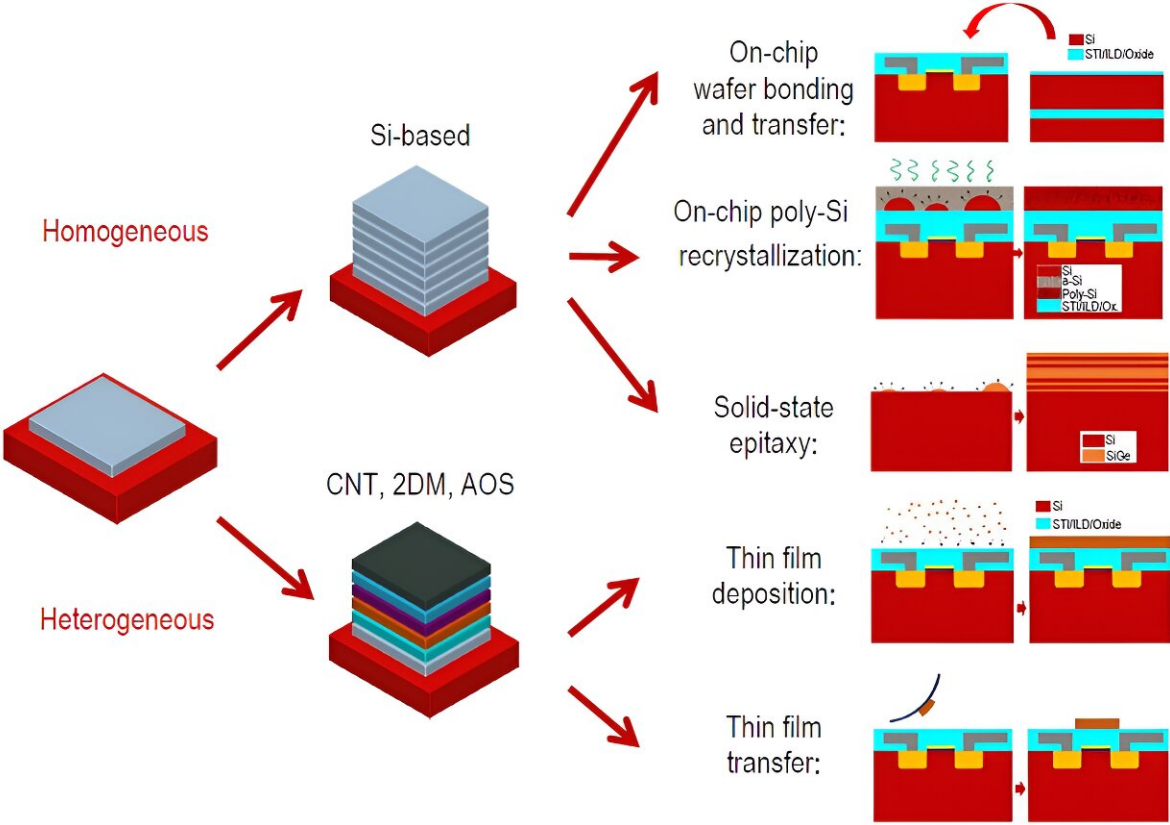
A review [published](#) in the journal *National Science Review* summarizes the research of a team led by Prof. Huaxiang Yin (Institute of Microelectronics of Chinese Academy of Sciences). They systemically reviewed the development history of Si-based metal-oxide-semiconductor field-effect-transistors (MOSFETs), including the theory update, new materials introduction, key processes breakthrough, especially on device structure innovations for the development of advanced integrated circuits (ICs) in the past twenty years.

The structure of the Si-based transistors would be changed from the fin field-effect transistor (FinFET) to the cutting-edge Stacked NanoSheet/NanoWire Gate-All-Around FETs (GAAFETs) at 3 nm node. Therefore, they introduce up-to-date GAAFET integration process methods and the recent technical progress in research institutions and IC industries.

Furthermore, the key challenges in fabricating the GAAFETs are illustrated in detail, including high-quality GeSi/Si superlattice periodic epitaxy, channel release, inner spacer module, SD-selective epitaxial defects, parasitic sub-fin channel leakage, HKMG filling, low hole mobility in the (100) orientation, [high voltage](#) (HV) and input/output (IO) integration, and high parasitic capacitance during AC operation. Some innovations in GAA devices, e.g., Forksheet FETs, Tree FET, Fishbone FET, and CombFET, are also introduced by the authors.

Beyond GAAFETs, CFETs, also known as 3D Stacked FETs (3DS-FETs), are showing promise for scaling toward the 1 nm node. The

authors introduced two CFET integration process methods: sequential and monolithic CFETs. They analyzed the differences between these two kinds of CFET structures, their respective advantages, and the challenges in the fabrication process.



The introduction of new channel materials, such as carbon-based, two-dimensional, and amorphous oxide semiconductor materials (CNT, 2DM, AOS) enhance total performance of transistor 3D stacking and enable more flexible process and circuit design possibilities. Credit: Science China Press

In addition, the top layers using new channel materials, including CNTs, 2DMs, and AOSs with low-temperature processing characteristics, are becoming a trend of future 3D stacking technologies. Beyond device

structure and process breakthroughs, CFETs require a full DTCO or STCO to enable the construction of transistors, circuits, and even systems at various levels for higher PPA gain.

Except for horizontal and lateral conductance channels, the new paths of vertical GAAFETs (VGAAFET) have also been summarized, including vertical devices W. and W.O. self-aligned gates for 3DS-FETs. There are great advantages in continuous reduction in their contacted gate pitch (CGP), the SDC, and SRAM cell areas. Additionally, VGAAFETs also offer new opportunities for 3D integration in dynamic RAM (DRAM) and NOR-type memory applications.

Eventually, they summarized the critical challenges, such as precise process control at the [atomic level](#), incredible heat dissipation, and augmented parasitic capacitance/resistance during high-speed circuit operation, that need to be solved for vertical transistor 3D stacking applications in the mainstream IC industry.

They also provide insights into the future development pathways integrating transistor 3D stacking with new theory transistors like tunneling, negative capacitance, and quantum devices in innovative monolithic 3D chips and systems. The review has significant guidance for advanced IC manufacturing, modeling, and design areas for 3 nm nodes and beyond.

**More information:** Qingzhu Zhang et al, New structure transistors for advanced technology node CMOS ICs, *National Science Review* (2024). [DOI: 10.1093/nsr/nwae008](https://doi.org/10.1093/nsr/nwae008)

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