A new framework to improve high computing performance

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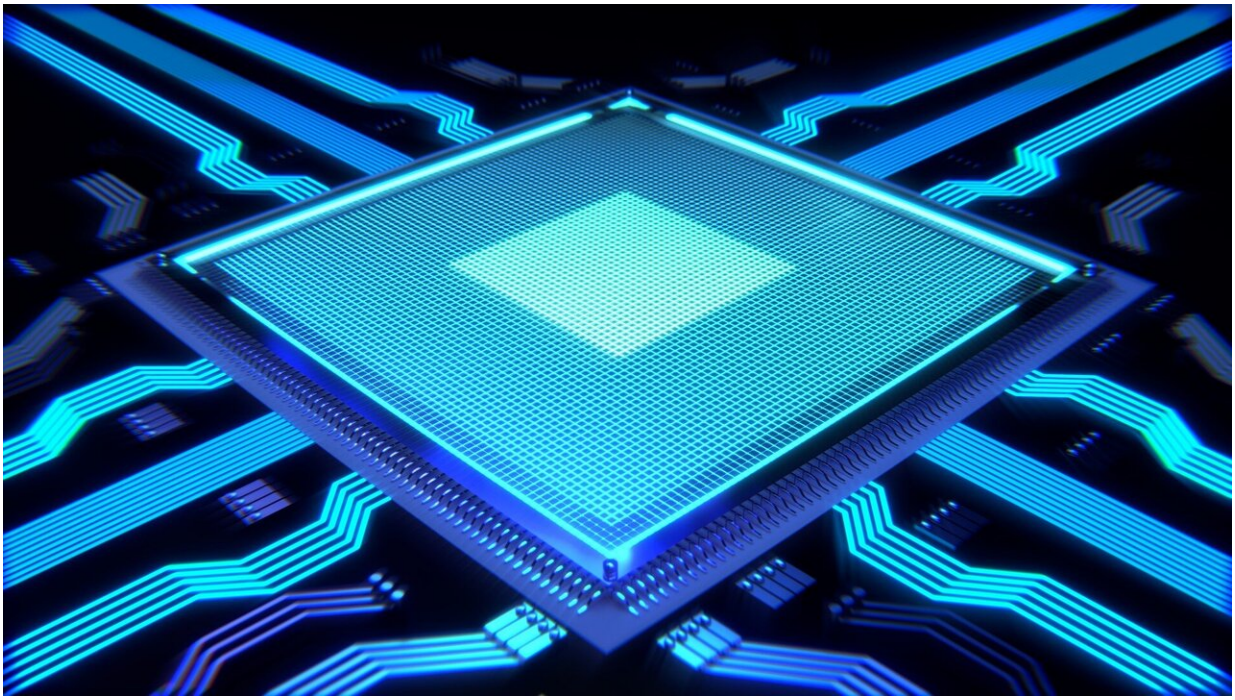

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From a luxury to a day-to-day necessity, computing isn't quite what it used to be. As applications like machine learning and 5G mobile networks become the norm, the need for high computing performance has never been greater. This has also necessitated the development of more energy-efficient and cost-effective systems like "chiplets" to help these applications run smoothly.

A chiplet is an unpackaged die that can be arranged into a package with other chiplets inside a chip. Each chiplet performs its own specific function. There are several approaches to chiplets, but the main idea is there is a menu of chiplets in a library. The chiplets are then assembled in a package and connected using a die-to-die interconnect scheme.

"The ever-growing on-package routing density and data rates of such serial links inevitably lead to more complex and worse signal and power integrity issues than a large monolithic chip," explained Jingtong Hu, associate professor of electrical and computer engineering and William Kepler Whiteford Faculty Fellow at the University of Pittsburgh Swanson School of Engineering. "This demands more efficient analysis and validation tools to support robust design."

To meet these demands, Hu and his team have developed SPIRAL, a framework for signal-power integrity co-analysis of high-speed interchiplet serial links. The work is published as part of the *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)*.

SPIRAL builds equivalent models for the links with a machine-learning based transmitter model and an impulse response based model for the channel and receiver. Then, the single-power integrity is co-analyzed with a pulse response based method using equivalent methods.

SPIRAL is an improvement over the Simulation Program with Integrated Circuit Emphasis (SPICE), a general purpose, open source integrated simulator used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

"Existing SPICE doesn't provide accurate analysis and validation for Chiplet since it is a really new technology," Hu said. "SPIRAL is trying to fill this gap and provide that."

More information: Xiao Dong et al, SPIRAL: Signal-Power Integrity Co-Analysis for High-Speed Inter-Chiplet Serial Links Validation, *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)* (2024). DOI: 10.1109/ASP-DAC58780.2024.10473908

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