RVAM16: A low-cost multiple-ISA processor based on RISC-V and ARM thumb

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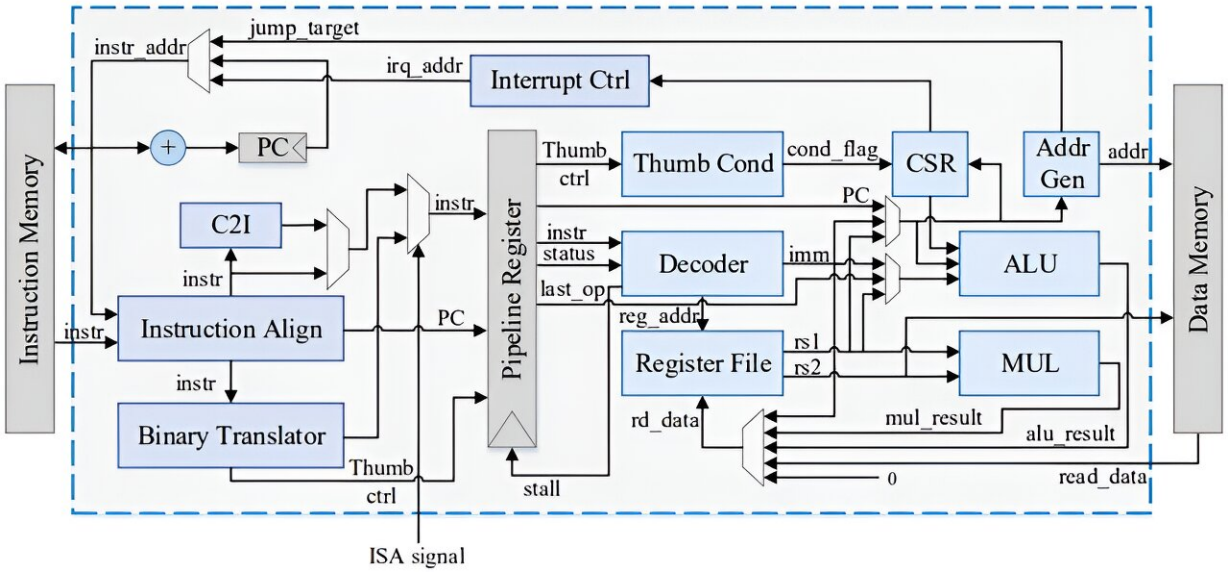

Credit: Libo Huang , Jing Zhang , Ling Yang , Sheng Ma , Yongwen Wang , Yuanhu Cheng

The increasing demand in the embedded field has led to the emergence of several impressive Instruction Set Architectures (ISAs). However, when processors migrate from one ISA to another, software compatibility issues are unavoidable.

Despite the availability of software binary translation systems for ensuring software compatibility, these systems have limitations (e.g.

performance and power) in low-cost embedded systems.

Targeting two of the most popular ISAs in the embedded field, RISC-V and ARM Thumb, research team led by Professor Libo Huang proposed RVAM16, a multiple-ISA processor based on hardware binary translation, as a solution to address software compatibility. The multiple-ISA processor not only avoids the startup and additional run time of software DBT systems but also can directly execute all non-native ISA programs, which does not suffer the dilemma of SBT.

By hardware optimization techniques for the ARM Thumb conditional flags, branch instructions, and conditional execution instructions in the RISC-V pipeline, RVAM16 significantly reduces the performance gap between running native ISA programs and non-native ISA programs in HBT-based multiple-ISA processors. Moreover, To keep the area and power consumption of RVAM16 within acceptable limits, the research team designed the 32-bit processor using time-sharing multiplexing the 16-bit data path technology.

The research also implemented and evaluated a prototype processor of RVAM16 that supports both RV32IMC and ARMv6-M. The evaluation results show that, when running non-native ARM Thumb programs, RVAM16 achieves a significant speedup of over 2.73x compared to using hardware binary translation alone, reaching more than 70% of the performance of native RISC-V programs. On the other hand, RVAM16 is also comparable in area and power compared to traditional single-ISA processors with similar features.

Furthermore, with suitable adaptations to the binary translator and related hardware optimization units, the proposed architecture can be effectively harnessed to accommodate any pair of distinct ISAs.

This flexibility positions the RVAM16 microarchitecture as a

compelling and versatile solution for addressing the challenges of software compatibility stemming from diverse ISAs.

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More information: RVAM16: a low-cost multiple-ISA processor based on RISC-V and ARM Thumb, *Frontiers of Computer Science* (2024). DOI: 10.1007/s11704-023-3239-x.
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