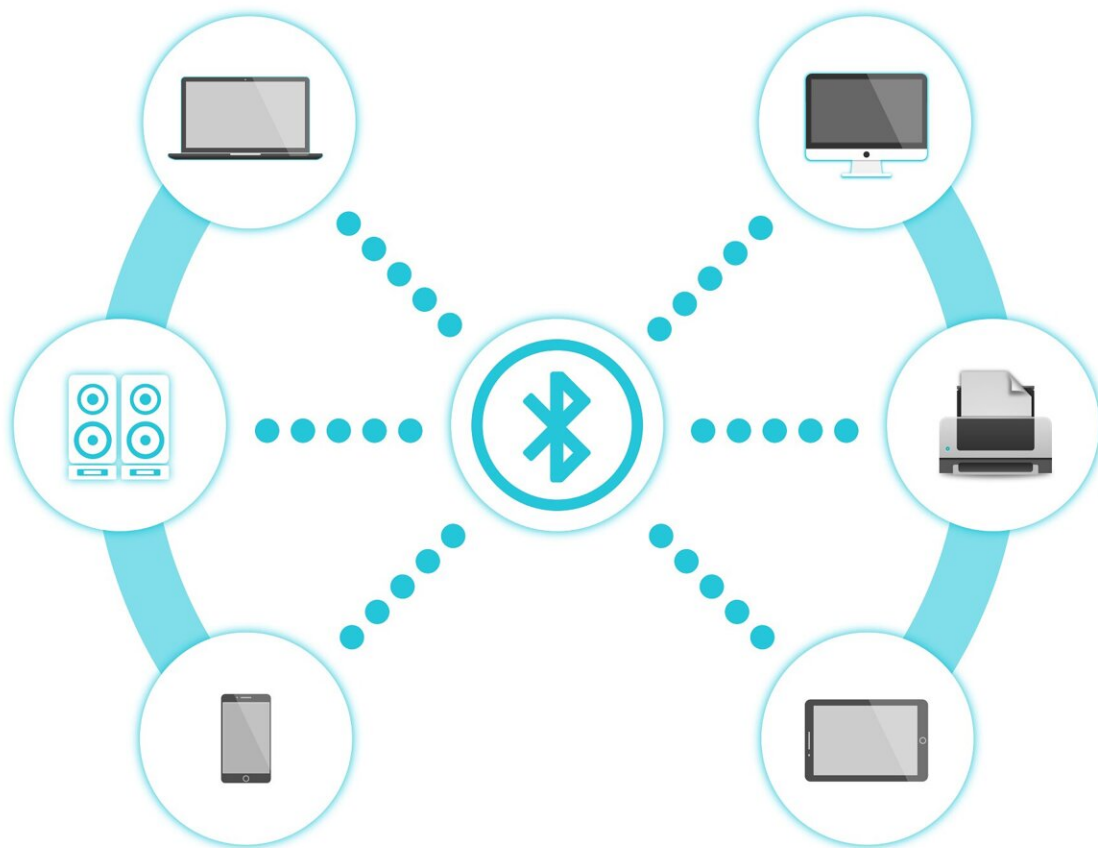# Researchers and industry partners demonstrate cutting-edge chip technology for ultra-low power AI connected devices

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Researchers from NUS, together with industry partners Soitec and NXP Semiconductors, have demonstrated a new class of silicon systems that promises to enhance the energy efficiency of AI connected devices by leaps and bounds. These technological breakthroughs will significantly advance the capabilities of the semiconductor industry in Singapore and beyond.

This innovation has been demonstrated in fully-depleted silicon-on-insulator (FD-SOI) technology, and can be applied to the design and fabrication of advanced semiconductor components for AI applications.

The new chip technology has the potential to extend the battery life of wearables and smart objects by a factor of 10, support intense computational workloads for use in Internet of Things applications, and halve the power consumption associated with wireless communications with the cloud.

The new suite of disruptive chip technologies will be promoted through the FD-SOI & IoT Industry Consortium to accelerate industry adoption by lowering the design barrier to entry in FD-SOI chips.

An industry workshop titled "Next-gen energy-efficient FD-SOI systems" was held on 3 May 2024 for participants from the industry and research community to share and discuss the latest developments in FD-SOI technologies, and showcase the new capabilities with state-of-the-art demonstrations.

"IoT devices often operate on a very limited power budget, and hence require extremely low average power to efficiently perform regular tasks such as physical signal monitoring," said Professor Massimo Alioto, who is from the NUS College of Design and Engineering's Department of Electrical and Computer Engineering and is also the Director of the FD-fAbrICS (FD-SOI Always-on Intelligent & Connected Systems) joint lab

where the new suite of technologies was engineered.

"At the same time, high peak performance is demanded to process occasional signal events with computationally-intensive AI algorithms. Our research uniquely allows us to simultaneously reduce the average power and improve the peak performance.

"The applications are wide-ranging and include smart cities, smart buildings, Industry 4.0, wearables and smart logistics. The remarkable energy improvements obtained in the FD-fAbrICS program are a game changer in the area of battery-powered AI devices, as they ultimately allow us to move intelligence from conventional cloud to smart miniaturized devices," said Prof Alioto, who also heads the Green IC group (www.green-ic.org) at the Department of Electrical and Computer Engineering.

Powering AI devices with ultra-energy efficient chips

Research conducted by the NUS FD-fAbrICS joint lab showed that their FD-SOI chip technology can be deployed at scale with enhanced design and system integration productivity for lower cost, faster market reach, and rapid industry adoption.

"This innovation has the potential to accelerate the time to market for key players in Singapore's semiconductor ecosystem," said Prof Alioto.

"We hope to facilitate the adoption and deployment of our design technologies at scale through the FD-SOI & IoT Industry Consortium. This is a significant contribution to the AI and semiconductor industry in Singapore, as it enables a competitive advantage while reducing the overall development cost of FD-SOI systems."

The research breakthroughs from the NUS FD-fAbrICS joint lab

leverage the combined NUS expertise and capabilities from different domains, such as digital circuits (Prof Massimo Alioto), wireless communications (Assoc Prof Heng Chun Huat), system architectures (Asst Prof Trevor Carlson), and AI models (Prof Li Haizhou). Industry leaders such as Soitec, NXP and Dolphin Design contributed to the research efforts at the joint lab, which is also supported by the Agency for Science, Technology and Research.

The NUS research team is now looking into developing new classes of intelligent and connected silicon systems that could support larger AI model sizes ("large models") for generative AI applications. The resulting decentralization of AI computation from cloud to distributed devices will simultaneously preserve privacy, keep latency at a minimum, and avoid wireless data deluge under the simultaneous presence of a plethora of devices.

Accelerating industry adoption of FD-SOI technologies

The industry workshop, which delved into the cutting-edge advancements and applications of FD-SOI technology, aimed to foster an environment of knowledge sharing as well as catalyze collaborations within, and between, the FD-SOI research community and the semiconductor industry in Singapore working on intelligent and connected silicon systems.

Another objective of the workshop was to facilitate rapid FD-SOI adoption and lower the design barrier to entry, by sharing the research outcomes from the FD-fAbrICS joint lab. Speakers from Soitec, GlobalFoundries, NXP, and the NUS FD-fAbrICS research team shared their perspectives on the current development of related technologies—for example, in manufacturing and microchip

design—and future disruptive technologies for next-generation ultra-low power AI systems.

FD-SOI & IoT industry Consortium

The FD-SOI & IoT Consortium was established to extend the impact of the NUS FD-fAbrICS joint lab on the semiconductor ecosystem in Singapore. Soitec and NXP are founding members of the Consortium.

Consortium members will have access to innovative FD-SOI design IP and methodologies, which will help to accelerate their next-generation prototyping and development cycle with highly energy efficient processes, especially in the fast-growing area of AI-connected chips.

The FD-SOI & IoT Consortium will support the near-term needs of industry for rapid technology road mapping and accelerated innovation cycle. At the same time, to assure sustained scalability and differentiation across the Consortium members in the longer term, the technologies developed in synergy with the FD-fAbrICS industry partners will be further expanded by some of the Consortium members.

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