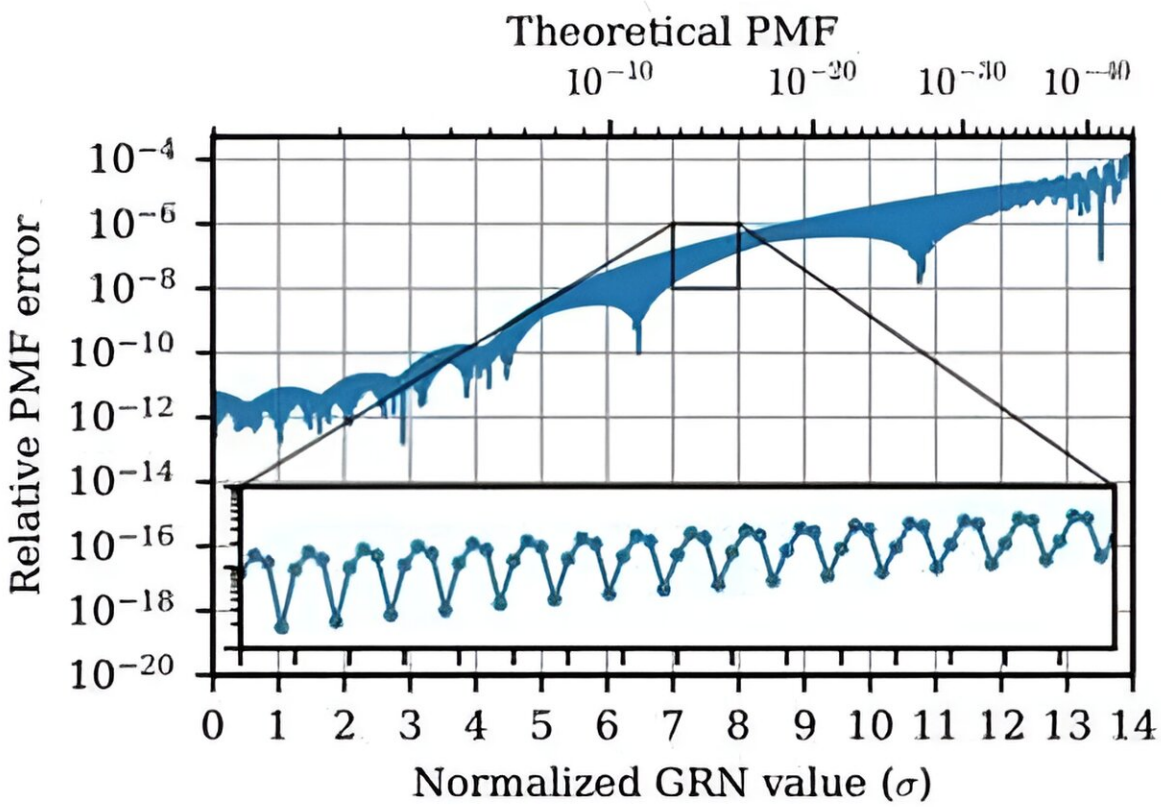
Researchers propose design methodology for hardware Gaussian random number generators

May 6 2024



Maximum relative PMF error versus σ value, with scaling index introduced. Credit: Zhuo Chen, USTC

A research team from the University of Science and Technology of China (USTC) of the Chinese Academy of Sciences (CAS) has proposed a novel design methodology for Gaussian random number (GRN) generators tailored for SerDes simulation systems.

The study was published in *IEEE Transactions on Circuits and Systems I: Regular Papers*.

Additive white Gaussian noise (AWGN) serves as a standard model for encapsulating the combined impact of various random and unpredictable noise sources. Consequently, GRN generators, capable of producing AWGN as hardware modules, play an important role in numerous high-performance hardware simulation systems.

Since the pioneering implementation of the Box-Muller algorithm in hardware back in 2000, research into hardware GRN generation algorithms has flourished. However, for hardware systems, traditional algorithms often necessitate additional multipliers and rounding units, leading to increased hardware consumption and error sources.

Moreover, the output range designed via traditional methods typically requires post-design testing or theoretical analysis for determination. Direct means for expanding the output range is lacking.

Based on the relatively novel Piecewise-CLT algorithm, the team proposed a novel design approach for GRN generators capable of accommodating arbitrary σ values and output ranges, which was achieved by introducing variable σ values and pre-defined GRN output ranges into the algorithmic expression derivation process. Utilizing this approach, the team crafted a generator boasting a theoretical output range of ±14σ.

However, the team's attempts to introduce reconfigurability into the

algorithm faced a challenge; directly reconfiguring the σ value of the existing hardware architecture led to increased errors as σ decreased, severely limiting practicality. Therefore, a parameter termed the scaling index was introduced to the algorithm.

This parameter enabled the algorithm to adjust relevant values differently based on varying σ values during random number generation, resulting in a relatively stable error curve and facilitating real-time configuration of σ values.

Based on the above findings, the team proposed a novel design methodology for hardware GRN generators. Compared to traditional approaches, this method offers superior flexibility and usability by supporting arbitrary σ values, arbitrary output ranges, and reconfigurability.

It stands poised to underpin the development of high-performance hardware simulation systems characterized by higher clock speeds, increased degrees of parallelism, and enhanced hardware resource utilization rates.

More information: Zhuo Chen et al, Flexible FPGA Gaussian Random Number Generators With Reconfigurable Variance, *IEEE Transactions on Circuits and Systems I: Regular Papers* (2024). DOI: 10.1109/TCSI.2024.3374731

Provided by University of Science and Technology of China