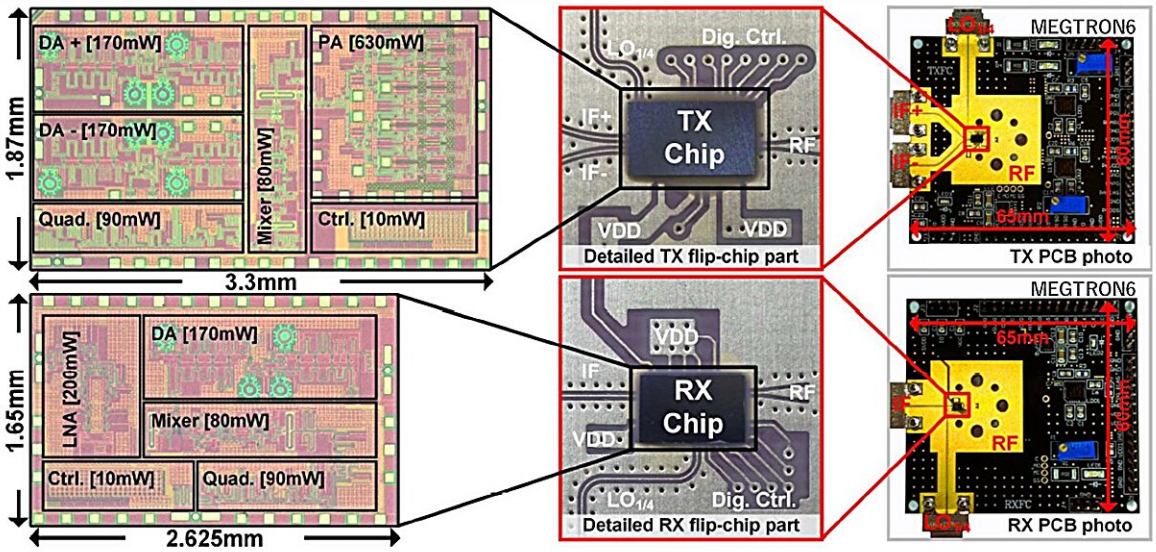
A novel 640 Gbps chipset paves the way for next generation wireless systems

June 17 2024



The fabricated D-band transmitter/receiver chipset: (Top) Transmitter, (Bottom) Receiver,(Left) CMOS transmitter/receiver IC, (Middle) Flip-chip mounted IC chip, and (Right) Entire board. Credit: The 2024 IEEE Symposium on VLSI Technology & Circuits

A new D-band CMOS transceiver chipset with 56 GHz signal-chain bandwidth achieves the highest transmission speed of 640 Gbps for a wireless device realized with integrated circuits, as reported by researchers from Tokyo Tech and National Institute of Information and Communications Technology. The proposed chipset is highly promising

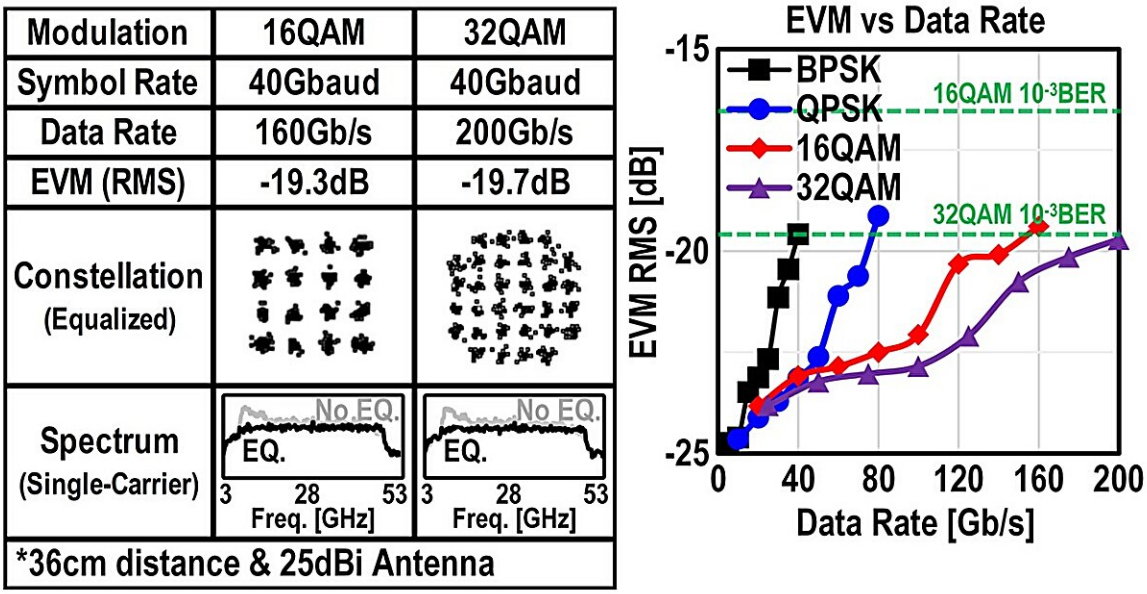
for the next generation of wireless systems.

To achieve faster speeds and handle increasing data traffic, wireless systems are operating in higher millimeter-wave frequency bands. Current high-band 5G systems offer speeds as high as 10 Gbps and operate in frequency bands between 24–47 GHz. The next generation of mobile communication systems, is exploring even higher frequency bands.

Within this spectrum, the D-band, covering frequencies from 110 to 170 GHz, is expected to play a crucial role in the development of next generation of wireless systems. While high frequencies provide faster data speeds, they are susceptible to attenuation. Therefore, for the widespread adoption of next generation of wireless systems, cost-effective transmitters and receivers capable of maintaining signal strength are crucial.

Recently, Professor Kenichi Okada and his team at Tokyo Institute of Technology, in collaboration with National Institute of Information and Communications Technology (NICT), Japan, have developed a novel transceiver chipset for the D-band. This chipset is fabricated using the widely-used 65nm silicon Complementary Metal-Oxide-Semiconductor (CMOS) process, making it cost-effective for mass production.

The research results are being presented at the 2024 IEEE Symposium on VLSI Technology & Circuits, June 16–20 in Honolulu, U.S..



Results of wireless transmission measurement at a short distance (36 cm). Credit: The 2024 IEEE Symposium on VLSI Technology & Circuits

Okada said, "Notably, the world's highest wireless transmission rate of 640 Gbps is achieved using low-cost CMOS technology."

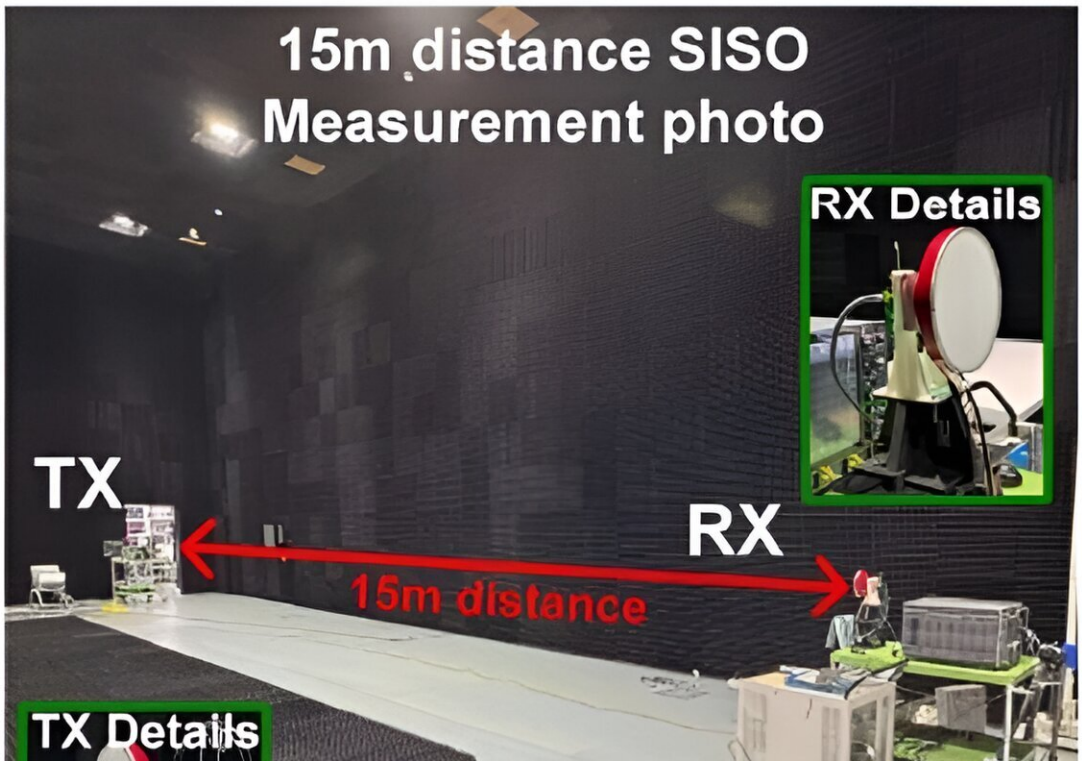
This work presents a D-band (114–170 GHz) CMOS transceiver chipset covering a 56 GHz signal-chain bandwidth. The transceiver, with a chip size of 1.87 mm x 3.30 mm for the transmitter integrated circuit (IC) and 1.65 mm x 2.60 mm for the receiver IC, uses components designed to maintain signal speed and quality across a broad frequency spectrum.

These include power amplifiers for elevating signals to suitable levels, low-noise amplifiers for boosting signal strength while minimizing noise, frequency converters (mixers) for adjusting signals to the desired frequency range, distributed amplifiers for linearity, and frequency multipliers for quadrupling the frequency.

To assess the wireless transmission capabilities, the researchers mounted the chipset on a PCB and connected it to an external antenna with a gain of 25 dBi. The signal was converted from a transmission line format, typically used on PCBs, to a waveguide format, used for high-frequency signal transmission in wireless applications, with the conversion loss kept to 4 dB.

With the new chipset, the researchers achieved high linearity for multi-level modulation schemes like 16QAM and 32QAM (QAM: Quadrature Amplitude Modulation), solving a major roadblock for IC transceivers.

In testing with a modulated signal with a symbol rate of 40 Gbaud and 32QAM modulation at a distance of 36 cm, the system achieved a transmission speed of 200 Gbps with high modulation accuracy, with a bit error rate of less than 10^{-3}. Furthermore, using 16QAM modulation and a high-gain antenna (with a gain of 43 dBi), the researchers were able to achieve speeds of 120 Gbps over a distance of 15 m.



A photo depicting the single-input single-output measurement at a transmission distance of 15 m in B5G anechoic chamber building of NICT. Credit: The 2024 IEEE Symposium on VLSI Technology & Circuits

The chipset's performance was further impressive in a multiple-input multiple-output configuration with four transmitters and four receiver modules. Here, each antenna can handle its own data stream, enabling fast communication. Using 16QAM modulation, each channel reached a speed of 160 Gbps. Overall, this resulted in a total speed of 640 Gbps.

These speeds represent a significant leap, being 10 to 100 times faster than current 5G systems. Okada concludes, "The proposed chipset holds promise for the next generation of wireless systems to support automated cars, telemedicine, and advanced virtual reality experiences."

More information: Presentation: A 640-Gb/s 4×4-MIMO D-Band CMOS Transceiver Chipset

Provided by Tokyo Institute of Technology