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Researchers enhance performance of hafnia-based memory devices by doping ferroelectric materials with aluminum

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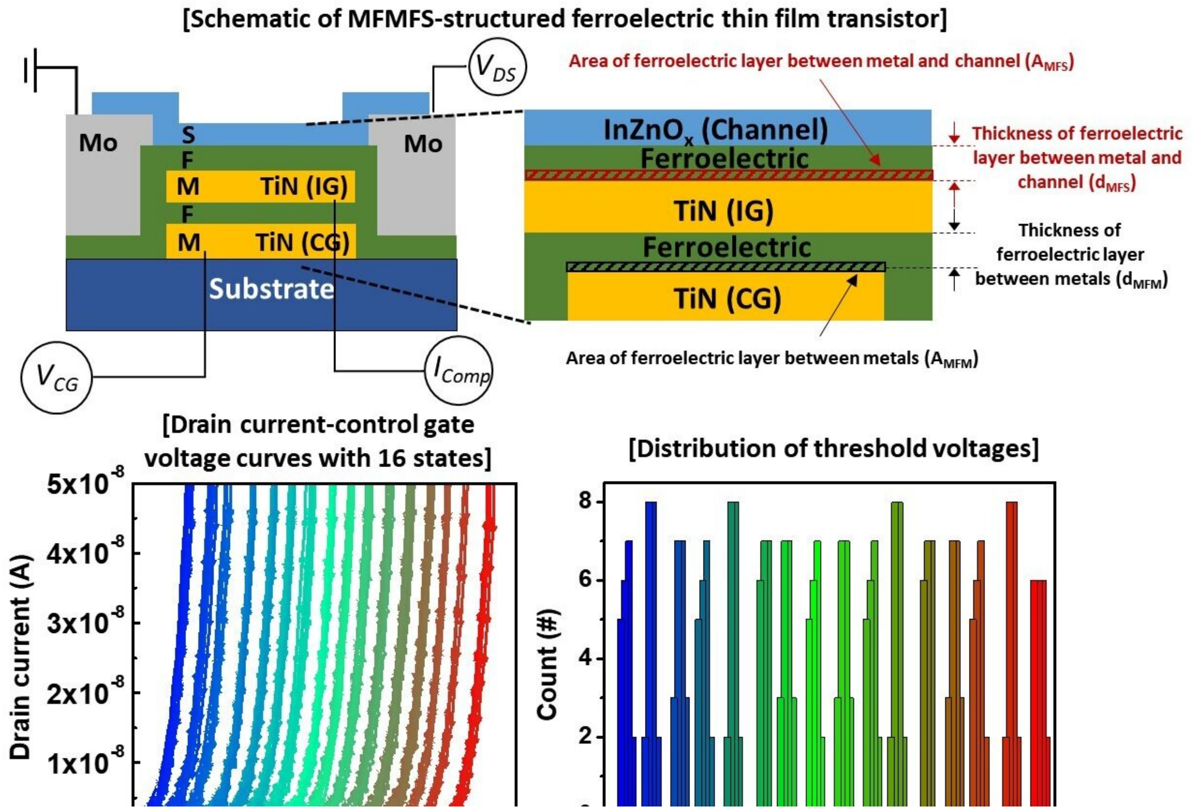

Schematic of the ferroelectric memory device, showing QLC behavior and the operation method. Credit: POSTECH

A research team has significantly enhanced the data storage capacity of ferroelectric memory devices. By utilizing hafnia-based ferroelectric materials and an innovative device structure, their findings, published on June 7 in the journal *Science Advances,* mark a substantial advancement in memory technology. The team was led by Professor Jang-Sik Lee from the Department of Materials Science and Engineering and the Department of Semiconductor Engineering at Pohang University of Science and Technology (POSTECH).

With the exponential growth in data production and processing due to advancements in electronics and artificial intelligence (AI), the importance of data storage technologies has surged. NAND flash memory, one of the most prevalent technologies for mass data storage, can store more data in the same area by stacking cells in a three-dimensional structure rather than a planar one. However, this approach relies on charge traps to store data, which results in higher operating voltages and slower speeds.

Recently, hafnia-based ferroelectric memory has emerged as a promising next-generation memory technology. Hafnia (Hafnium oxide) enables ferroelectric memories to operate at low voltages and high speeds. However, a significant challenge has been the limited memory window for multilevel data storage.

Professor Lee's team at POSTECH has addressed this issue by introducing new materials and a novel device structure. They enhanced the performance of hafnia-based memory devices by doping the ferroelectric materials with aluminum, creating high-performance ferroelectric thin films.

Additionally, they replaced the conventional metal-ferroelectric-

semiconductor (MFS) structure, where the metal and ferroelectric materials that make up the device are simply arranged, with an innovative metal-ferroelectric-metal-ferroelectric-semiconductor (MFMFS) structure.

The team successfully controlled the voltage across each layer by adjusting the capacitance of the ferroelectric layers, which involved fine-tuning factors such as the thickness and area ratio of the metal-to-metal and metal-to-channel ferroelectric layers. This efficient use of applied voltage to switch ferroelectric material improved the device's performance and reduced energy consumption.

Conventional hafnia-based ferroelectric devices typically have a memory window of around 2 volts (V). In contrast, the research team's device achieved a memory window exceeding 10 V, enabling Quad-Level Cell (QLC) technology, which stores 16 levels of data (4 bits) per unit transistor. It also demonstrated high stability after more than one million cycles and operated at voltages of 10 V or less, significantly lower than the 18 V required for NAND flash memory. Furthermore, the team's memory device exhibited stable characteristics in terms of data retention.

NAND flash memory programs its memory states using Incremental Step Pulse Programming (ISPP), which leads to long programming times and complex circuitry. In contrast, the team's device achieves rapid programming through one-shot programming by controlling ferroelectric polarization switching.

Professor Lee of POSTECH commented, "We have laid the technological foundation for overcoming the limitations of existing memory devices and provided a new research direction for hafnia-based ferroelectric memory." He added, "Through follow-up research, we aim to develop low-power, high-speed, and high-density memory devices,

contributing to solving power issues in data centers and artificial intelligence applications."

More information: Ik-Jyae Kim et al, Unlocking large memory windows and 16-level data per cell memory operations in hafnia-based ferroelectric transistors, *Science Advances* (2024). DOI: 10.1126/sciadv.adn1345

Provided by Pohang University of Science and Technology

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