New 3D integrated metal-oxide transistors to fabricate compact and high density electronics

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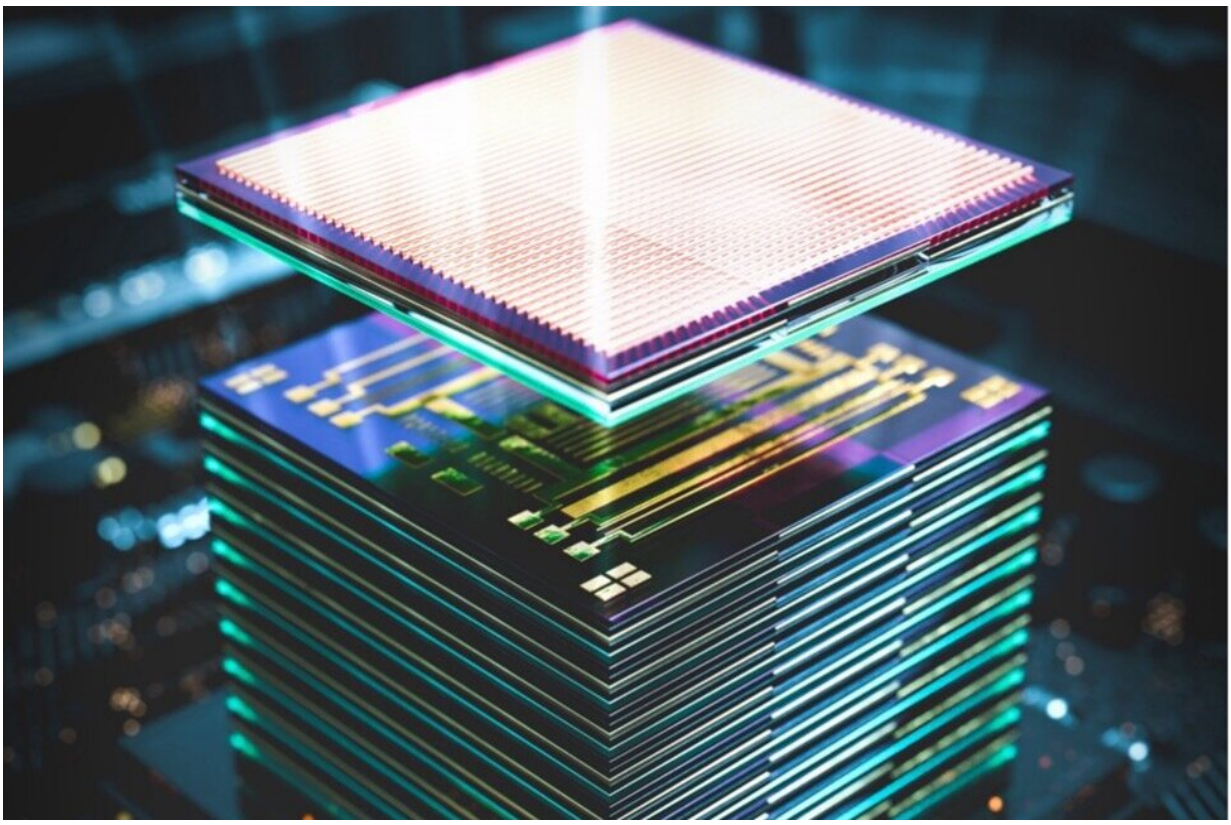

Artistic illustration of the 10-stacked metal oxide transistors. Credit: Yuvaraja et al.

Transistors are core components of many electronic devices, which serve

the role of amplifying and switching electrical signals. A key goal of the electronics industry is to continue improving the performance and energy-efficiency of transistors, while also reducing their size.

Researchers at King Abdullah University of Science and Technology (KAUST) have recently developed new three-dimensional (3D) integrated transistors that can be vertically stacked onto each other. Following their proposed design, introduced in a paper published in *Nature Electronics*, they were able to stack the highest number of transistors to date, which could translate in a significant boost in the performance of electronics.

"Our recent paper, which demonstrates the largest number of stacked metal oxide transistors in the world, originated from the pressing need to overcome the limitations of traditional planar transistors," Xiaohang Li, co-author of the paper, told TechXplore. "As technology evolves, the demand for more powerful, efficient, and compact electronic devices continues to grow. However, conventional planar transistors are reaching their physical and performance limits, which restricts their ability to meet these demands. This is also known as the slowing down of Moore's law."

Li and his colleagues have been working to overcome known challenges affecting the semiconductor industry, such as the slowing down of Moore's law and the search for new materials or designs that could further improve the performance of transistors. They have thus been exploring new and unique approaches that reach beyond the 2D layout of conventional transistors.

In their recent work, they have been particularly assessing the possibility of stacking the transistors vertically. This approach essentially entails the stacking of transistors on top of each other, which could increase transistor density and consequently also improve the performance of

electronics.

"The first objective of our study was to increase transistor density," Li explained. "By developing a technology with low thermal budget and low interfacial roughness, we have developed a 10-stack nanometer-thick compound semiconductor transistor; we aimed to maximize the use of wafer space. This vertical stacking approach allows for more transistors to be integrated into a given area, significantly enhancing processing power and efficiency."

The design introduced by this team of researchers entails stacking ten layers of indium oxide (In_2O_3) thin-film transistors (TFTs) vertically on CMOS-compatible silicon/silicon dioxide (Si/SiO_2) substrates. This vertical design maximizes the use of wafer space, resulting in a greater transistor density compared to planar designs.

"The transistors are arranged in a multi-layered structure, where each layer functions independently, but together they contribute to the overall performance," Li said. "We chose indium oxide (In_2O_3) for the semiconductor material due to its excellent electrical properties and compatibility with room temperature processing. For the dielectric layer, we selected parylene-C, which can be deposited at room temperature and provides effective insulation."

To fabricate their transistors, the researchers first deposited a thin layer of In_2O_3 on a silicon/silicon dioxide wafer. This deposited layer formed the channel through which electrical current flows.

"After the In_2O_3 layer, we deposited a layer of parylene-C," Li said. "This material serves as the dielectric, insulating each transistor layer and preventing electrical interference between layers."

Every layer within the team's transistor was patterned using an advanced,

72-step lithography-based process. This process is significantly more complex than the typical 10-step process used to pattern layers in simpler electronic structures.

"Each step required precise alignment and dose optimization to ensure the integrity and performance of each layer," Li explained.

The researchers repeated the deposition and patterning steps several times, until they stacked ten layers of transistors. Each of these layers was carefully aligned with the others to ensure the correct functioning of the device and connections between them.

The new vertical design introduced by this team of researchers enables a greater transistor density within a given area. This was found to translate into a greater processing power and efficiency.

"Both the In_2O_3 and parylene-C layers are processed at room temperature, making the fabrication process more energy-efficient and compatible with existing semiconductor manufacturing techniques," Li said. "The electrical characteristics of our transistors, including a maximum field-effect mobility of 15 $cm^2/V^{-1}s^{-1}$, a subthreshold slope of 0.4 V/dec^{-1}, and a current on/off ratio of up to 10^8, surpass those of many existing thin-film transistors. This results in faster switching speeds, lower power consumption, and improved overall performance."

The innovative transistor design introduced in this recent paper was so far used to develop high-performance and high-density transistors with ten vertical layers, yet their density could be scaled up further over time. The team's efforts could thus contribute to the further enhancement of electronics.

"Notably, both the In_2O_3 semiconductor and parylene-C dielectric materials can be processed at room temperature," Li said. "This is a

critical advancement as it makes the fabrication process more energy-efficient and compatible with existing semiconductor manufacturing techniques."

In initial tests, the transistors developed by Li and his colleagues achieved remarkable electronic performances, including a maximum field-effect mobility of 15 $cm^2/V^{-1}s^{-1}$, a subthreshold slope of 0.4 V/dec^{-1} and a current on/off ratio of up to 10^8. These metrics outperform those of many existing thin-film transistors, while also resulting in faster switching speeds and lower power consumption.

"Our technology can significantly benefit the mobile device industry by enabling the development of next-generation smartphones, tablets, and wearable devices with higher performance and longer battery life," Li said. "The IoT ecosystem also requires compact, energy-efficient devices capable of real-time data processing. Our transistors' high performance and low power consumption make them well-suited for various IoT applications, from smart homes to industrial automation."

A further application of the team's transistors could be in artificial intelligence (AI) and machine learning (ML). Training and deploying these computational tools requires substantial computational power and efficient data processing, which could be supported by the researchers' transistors.

"Beyond mobile devices, our technology can enhance a wide range of consumer electronics, including smart home devices, gaming consoles, and augmented/virtual reality (AR/VR) systems," Li said. "Improved performance and energy efficiency can lead to more responsive and immersive user experiences. Our 10-stack transistors can also contribute to the development of automotive electronics, providing the necessary computational power and reliability."

In the future, the vertically stacked transistors could also be used to develop more advanced and compact medical devices, such as diagnostic tools, biosensors, implantable technologies and wearable health monitors. Meanwhile, Li and his colleagues plan to explore other strategies to scale the transistors down further without compromising their performance.

"One of our primary objectives for future research will be to scale down the transistors from the current micron-scale to the nanoscale," Li added. "Achieving this will further increase transistor density, allowing for even higher performance and more compact device designs. We are also exploring new techniques and device topologies to reduce power consumption further, while also working to enhance the reliability and stability of our transistors, as this could facilitate their deployment."

More information: Saravanan Yuvaraja et al, Three-dimensional integrated metal-oxide transistors, *Nature Electronics* (2024). DOI: 10.1038/s41928-024-01205-0.

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