

Reconfigurable chaos-based microchips offer possible solution to Moore's law

20 September 2016, by Tracey Peake



Credit: North Carolina State University

Researchers at North Carolina State University have developed new, nonlinear, chaos-based integrated circuits that enable computer chips to perform multiple functions with fewer transistors. These integrated circuits can be manufactured with "off the shelf" fabrication processes and could lead to novel computer architectures that do more with less circuitry and fewer transistors.

Moore's law states that the number of transistors on an integrated circuit will double every two years in order to keep up with processing demands. Previously this goal has been addressed by shrinking the size of individual transistors so that more could be added to the chip. However, that solution is quickly becoming untenable, and the semiconductor industry is looking for new ways to create better computer chips.

"We're reaching the limits of physics in terms of transistor size, so we need a new way to enhance the performance of microprocessors," says Behnam Kia, senior research scholar in physics at NC State and lead author of a paper describing the work. "We propose utilizing chaos theory – the

system's own nonlinearity – to enable [transistor circuits](#) to be programmed to perform different tasks. A very simple nonlinear transistor circuit contains very rich patterns. Different patterns that represent different functions coexist within the nonlinear dynamics of the system, and they are selectable. We utilize these dynamics-level behaviors to perform different processing tasks using the same circuit. As a result we can get more out of less."

Kia and NC State colleague William Ditto, professor of physics and dean of the College of Sciences, worked on the conception, design, development and fabrication of an integrated circuit chip that contains working nonlinear circuits to perform multiple different digital computations.

Traditionally, transistor-based circuits perform one task each. Computer processors operate by routing each instruction and its operands to the appropriate transistor circuit on the integrated circuit that implements that specific instruction. In Kia's design, the transistor circuit can be programmed to implement different instructions by morphing between different operations and functions.

"In current processors you don't utilize all the circuitry on the processor all the time, which is wasteful," Kia says. "Our design allows the circuit to be rapidly morphed and reconfigured to perform a desired digital function in each clock cycle. The heart of the design is an analog nonlinear circuit, but the interface is fully digital, enabling the circuit to operate as a fully morphable digital circuit that can be easily connected to the other digital systems."

The researchers have produced an alternative approach for computing that is compatible with existing technology and utilizes the same fabrication process and CAD tools as existing computer chips, which could aid commercial adoption.

"We believe that this chip will help solve the challenges of demands for more processing power from fewer transistors," Kia says. "The potential of 100 morphable nonlinear chaos-based circuits doing work equivalent to 100 thousand circuits, or of 100 million transistors doing work equivalent to three billion transistors holds promise for extending Moore's law – not through doubling the number of transistors every two years but through increasing what transistors are capable of when combined in nonlinear and chaotic circuits."

"We are nearing commercial size and power and ease of programming in our evolving designs that could well be of significant commercial relevance within a few months with our three month design/fabrication cycle of improvements and implementations," Ditto says.

The work appears in *IEEE Transactions on Circuits and Systems II: Express Briefs*. Kenneth Mobley of FirstPass Engineering also contributed to the work.

More information: Behnam Kia et al. An Integrated Circuit Design for a Dynamics-Based Reconfigurable Logic Block, *IEEE Transactions on Circuits and Systems II: Express Briefs* (2016).
[DOI: 10.1109/TCSII.2016.2611442](https://doi.org/10.1109/TCSII.2016.2611442)

Provided by North Carolina State University

APA citation: Reconfigurable chaos-based microchips offer possible solution to Moore's law (2016, September 20) retrieved 17 June 2021 from <https://techxplore.com/news/2016-09-reconfigurable-chaos-based-microchips-solution-law.html>

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