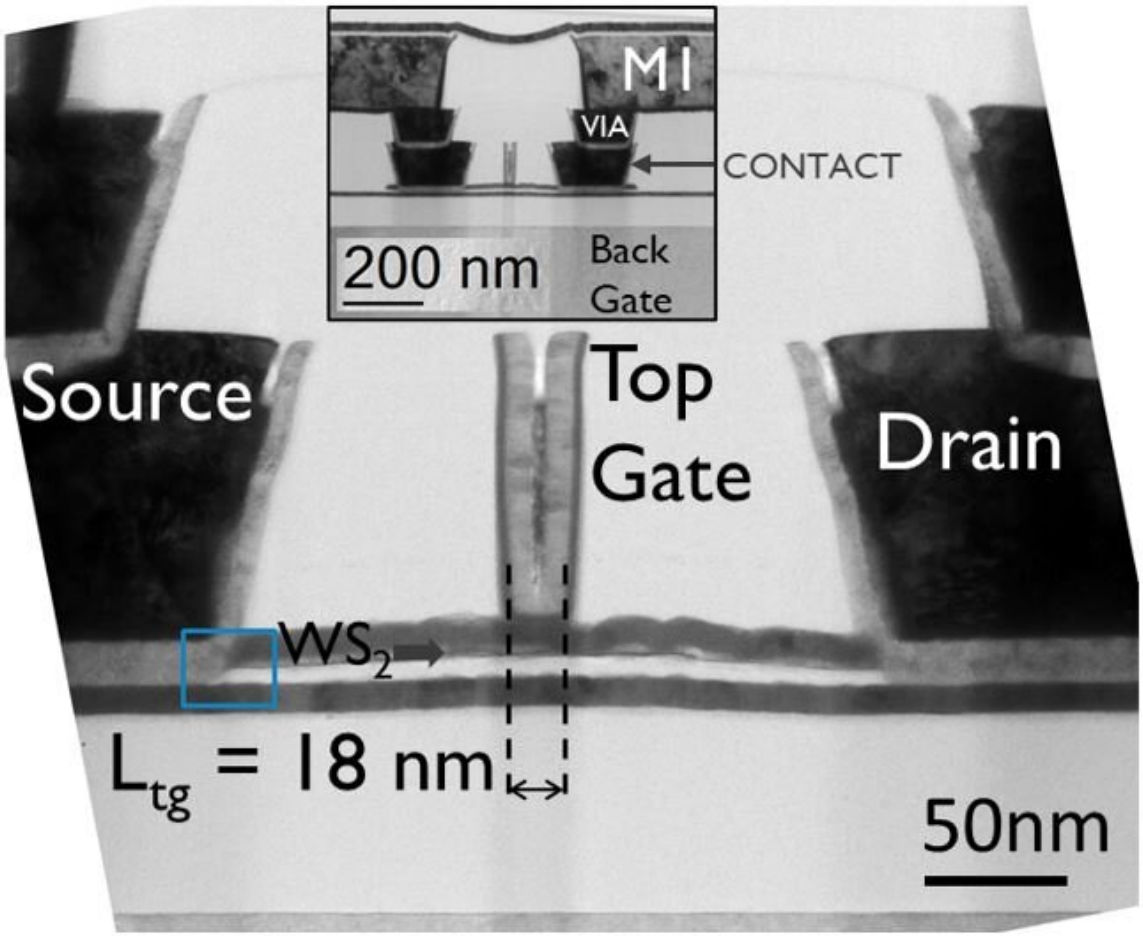
Imec introduces 2-D materials in the logic device scaling roadmap

January 12 2021, by Iuliana Radu, Zuhair Ahmed, Inge Asselberghs , Dennis Lin and Quentin Smets



TEM image of a 2D device fabricated with 300mm processes. Credit: imec

The continual scaling of Si-based transistors is challenged by short channel effects that limit further gate length scaling. Field-effect transistors (FETs) with semiconducting transition metal dichalcogenides (MX2, such as WS_2 or MoS_2) as the semiconductor channel promise however to be relatively immune to these short channel effects. FETs with 2-D semiconductor channel owe this promise to the ability to make atomically thin channels combined with the theoretical ability to maintain higher carrier mobility—independent of channel thickness. These two properties give the gate voltage a better electrostatic control over the channel. Iuliana Radu, program director at imec, says, "2-D-FETs are considered prime candidates to further extend the logic device scaling roadmap. Our team at imec has set the scene for adopting these 2-D semiconductors into a 300mm integration flow—a key requirement for industrial adoption. We also obtained significant steps forward in improving device performance and in building fundamental understanding."

Extending the logic device scaling roadmap with 2-D-FETs: a DTCO analysis

"By using our design-technology co-optimization (DTCO) framework, we show how transistors with 2-D semiconductor channel can further extend the logic scaling roadmap," says Zubair Ahmed, imec researcher and first author of the paper on DTCO. "A circuit-level power-performance-area (PPA) evaluation at 2nm revealed for example that devices in a stacked 2-D-nanosheet configuration outperform their Si-based counterparts and have a reduced footprint." Within the model, the team used realistic assumptions as much as possible based on experimental data.

A 300mm platform for dual-gated 2-D-FETs

Several years ago, imec started pathfinding work on 300mm integration of both WS2- and MoS2-FET devices—a key requirement for industrial adoption. Inge Asselberghs, program manager of Exploratory Logic at imec and first author of the paper on 300mm integration: "This work has resulted in a unique 300mm test vehicle for 2-D-FETs, allowing the fabrication of functioning devices with gate lengths down to 18nm. The flow was used to study the impact of various processing conditions, such as the channel deposition and transfer process." The team also identified remaining challenges, including 2-D growth quality, formation of the gate dielectric, doping and contact resistance.

In the above-mentioned work, a dual-gated device structure was implemented. This is an important enabler for improved electrostatic control. "We showed experimentally that 2-D-FETs with connected top and back gate outperform single-gate counterparts in terms of drive current, transconductance and sub-threshold swing—important metrics for evaluating short-channel effects," explains Dennis Lin, principle scientist at imec and first author of the paper on dual-gated 2-D-FETs. The dual-gate concept also shows promise towards complementary MOS (CMOS) operation.

Sources of variability

The integration and device performance work were complemented with the first-ever variability study of a large set of nanoscale 2-D-FET devices. The team investigated various sources of variability—including the thickness of the 2-D-channel, the presence of bilayer islands and the 2-D growth template—and their respective impact on the electrical performance (mainly on the subthreshold regime). Quentin Smets, senior researcher at imec and first author of the 'variability' paper: "As a main conclusion, we found that variability can be strongly reduced if we thin down the 2-D-based channel to a single uniform monolayer. This is an encouraging result, as very thin channels will be needed for further

transistor scaling."

More information: Introducing 2D-FETs in device scaling roadmap using DTCO, Z. Ahmed et al. 2020 IEDM conference

Wafer-scale integration of double gated WS_2-transistors in 300mm Si CMOS fab, I. Asselberghs et al. 2020 IEDM conference

Dual gate synthetic WS_2 MOSFETs with 120μS/μm Gm 2.7μF/cm^2 capacitance and ambipolar channel, D. Lin et al. 2020 IEDM conference

Sources of variability in scaled MoS_2 FETs, Q. Smets et al. (IEDM highlight paper) 2020 IEDM conference

Provided by IMEC

Citation: Imec introduces 2-D materials in the logic device scaling roadmap (2021, January 12) retrieved 19 April 2024 from https://techxplore.com/news/2021-01-imec-d-materials-logic-device.html